FIREFLY_MGB
EH1702002012
Reference Manual

December 2018 ver1.1

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Revision History

Date	Rev	Comment
Nov 2017	v0	Initial version
Dec 2018	v1.1	Clock change to 212.5MHz and 100MHz

Contents

Dual FIREFLY Transceiver Card

IMPORTANT!

ESD

The FIREFLY_MGB Transceiver Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

- Transport the card in an ESD bag
- Wear an anti-static wrist strap
- Make sure the work area is equipped with an ESD mat

Warning

Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS® system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

Overview

This document is the FIREFLY_MGB Reference Manual and describes the functions of the FIREFLY_MGB interface card.

The Dual FireFly Transceiver Card (FIREFLY_MGB) includes two stacked FireFly transceiver connectors that support up to eight high-speed serial links over two FireFly cables that can be tuned to operate at up to 12.5Gbps per link with four links per connector socket.

Two on-board clock generators provide the FPGA Multi-Gigabit Transceiver (MGT) reference clocks. External clocks can also be brought in through FireFly connectors as the MGT reference clocks.

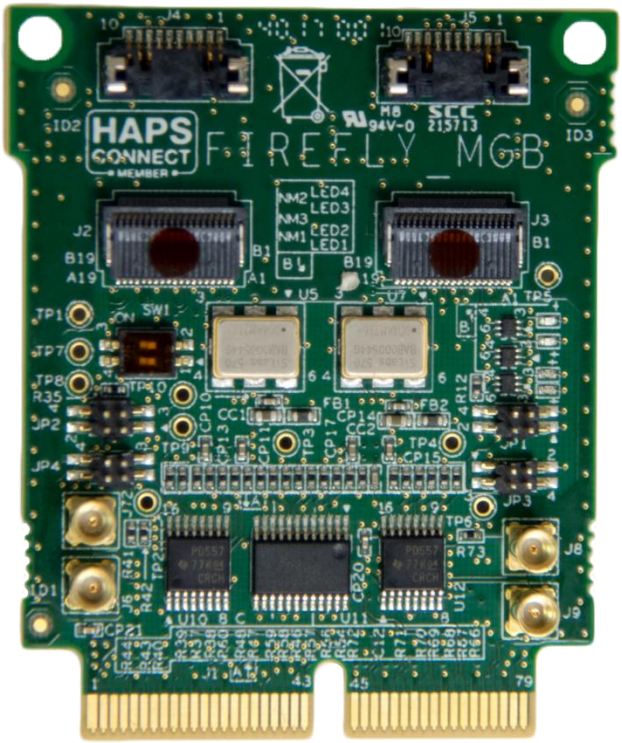


Figure 1: Top View of FIREFLY_MGB

Layout

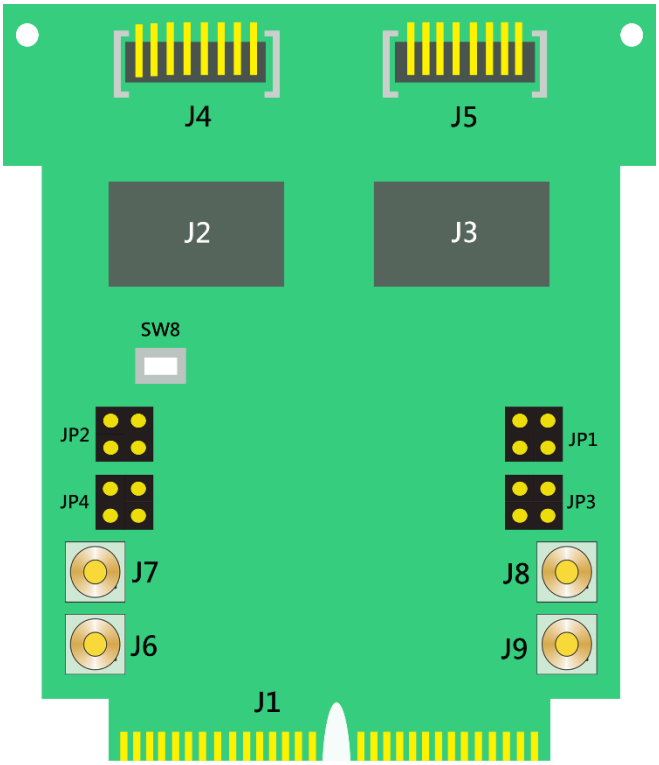


Figure 2: Top FIREFLY_MGB Card Layout

Block Diagram

FIREFLY_MGB is designed to provide flexibility in the configuration of the card for specific applications. The following block diagram and the accompanying I/O block diagram in Figure 4 depicts how functional blocks are interconnected.

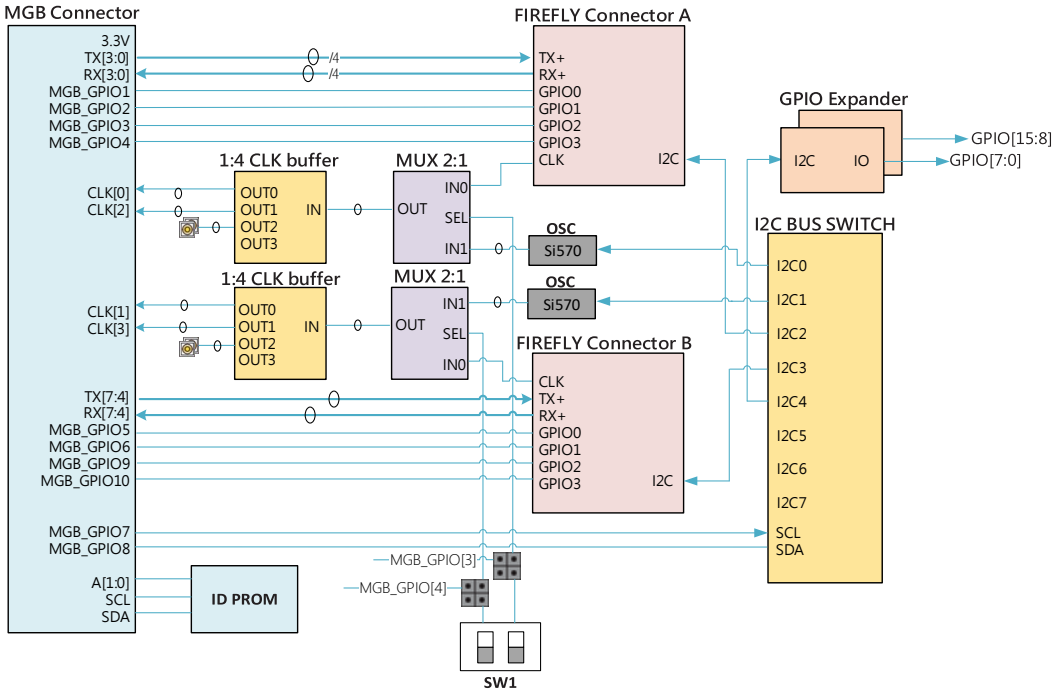


Figure 3: FIREFLY_MGB Architecture Block Diagram

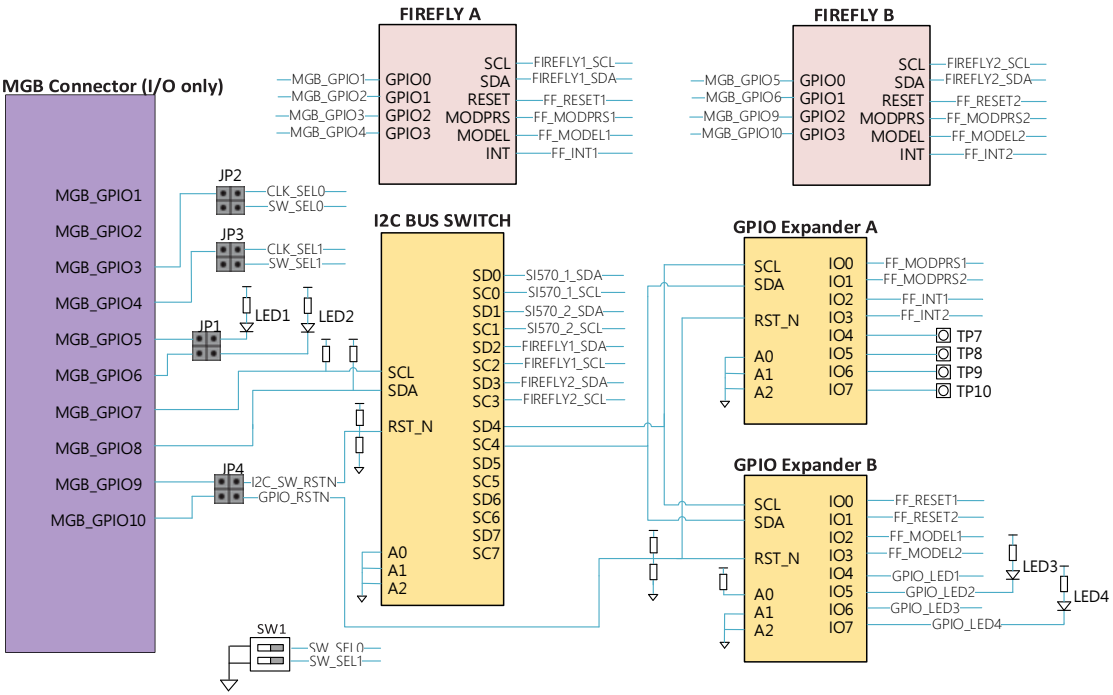


Figure 4: I/O Block Diagram

Card Placement

HAPS-80

HAPS-80 systems include two dedicated MGB connectors for each FPGA with eight GTH high-speed SerDes channels and 10 low-speed, general-purpose I/O signals on each connector. The MGB connectors appear at the back of specially designed compartments accessible from the sides of the HAPS-80 system. Slots in the brackets form shelves that provide the needed support for the MGB interface cards.

For more information about the available Synopsys MGB cards, go to synopsys.com or refer to the *HAPS MGB Interface Cards Reference Manual* at solvnet.synopsys.com.

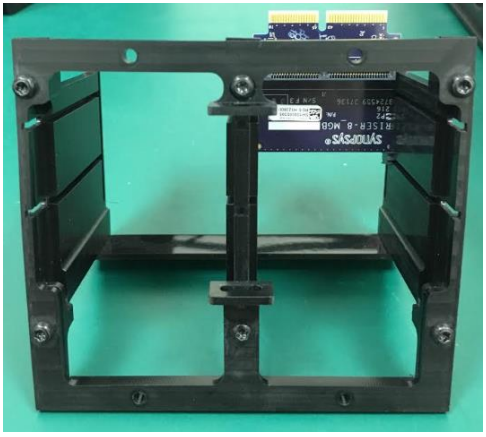
Figure 5: A FIREFLY_MGB Interface Card Installed on a HAPS-80

Mounting an MGB Interface Card

To mount the FIREFLY_MGB interface card in a HAPS-80 system:

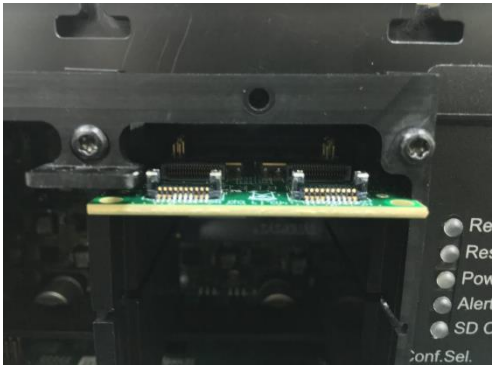
1. Remove the appropriate cage from The HAPS-80 chassis by removing the screws at the top and bottom and sliding the cage out of the compartment.

2. Insert the HAPS RISER8_MGB card, from the supplied hardware kit into one set of slots at the back of the cage. Make sure that the MGB interface connectors on the edge on the riser card are facing up and that the MGB card mating connectors are facing out. Each cage can hold two MGB cards.



3. Slide the cage back into the chassis and secure the cage to the chassis with the four screws previously removed. Reach into the cage and push the riser card up into its MGB mating connector located on the underside of the FPGA module. The riser card will “click” when properly seated.

4. Slide the FIREFLY_MGB interface card into the top set of slots and push firmly to seat the card connector into its mating connector on the riser card.



5. Insert the MGB container locking pin through its mounting holes in the top and bottom tabs on the cage as shown to secure the card or cards in place.

Clocks

Four reference clocks are available from two on-board oscillators:

CLK0 and CLK2: Default to 212.5MHz.Frequency control by MGB_GPIO7 and MGB_GPIO8 through I2C BUS SWITCH(P/N:PCA9548APW)

CLK1 and CLK3: Default to 100MHz.Frequency control by MGB_GPIO7 and MGB_GPIO8 through I2C BUS SWITCH(P/N:PCA9548APW)

In addition to the on-board oscillators, external differential clocks (FireFly connectors) can also be injected into the clock circuit. Select the external clock or on-board oscillator with slider switch SW1 or controlled through MGB_GPIO3 and MGB_GPIO4 by setting jumpers on headers JP2 and JP3. An MMCX differential clock output connector for each clock circuit is also available for clock export. The source of this clock can originate from either the local oscillator or from the external input.

When a switch is in the OFF position, the on-board oscillator is used. When a switch is in the ON position, the external reference clock is selected. See Figure 6.

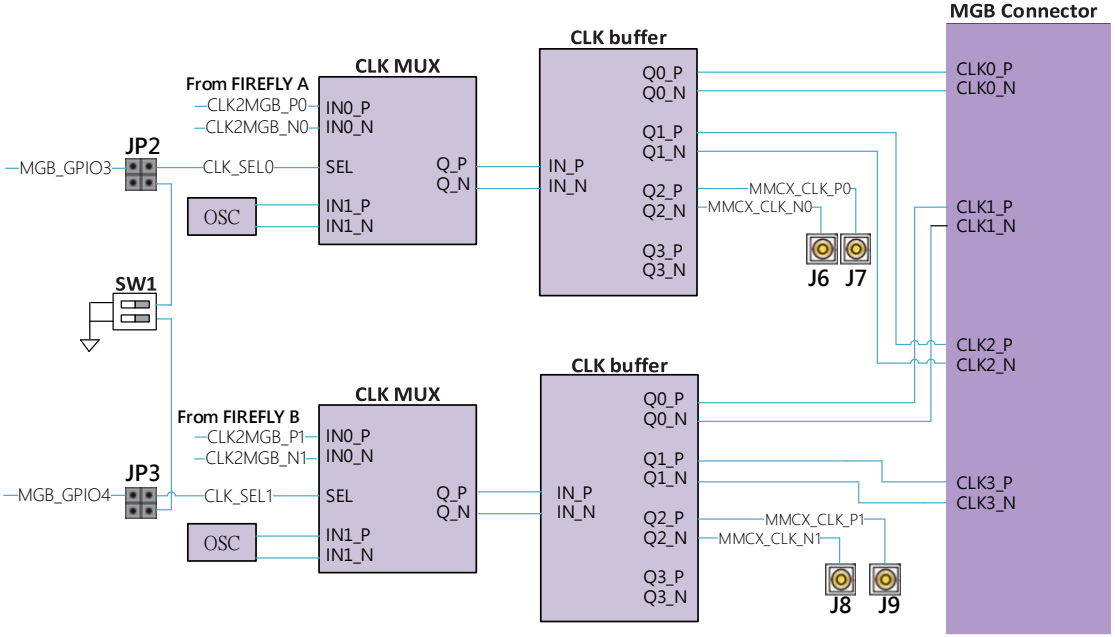


Figure 6: MGB Reference Clock Circuit

Jumpers and Switches

Jumpers provide different configuration options dependent on your requirements. The FIREFLY_MGB has four 2x2 jumpers. Refer to the I/O Block Diagram in Figure 4, on page 10.

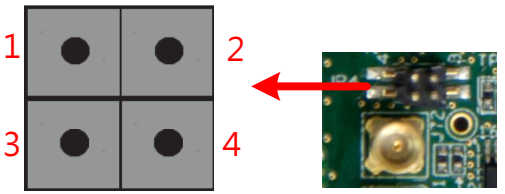


Figure 7: Header Strip

MGB header strip JP1-JP4 is populated by jumpers that connect the control signals (LED1, LED2, CLK_SEL0, CLK_SEL1, I2C_SW_RSTN and GPIO_RSTN) directly to MGB I/O signals. If these signals are not used to generate the control signals, the pins can be accessed for design-specific use directly from header JP1-JP4.

Switches SW1 select clock input based on user requirements.

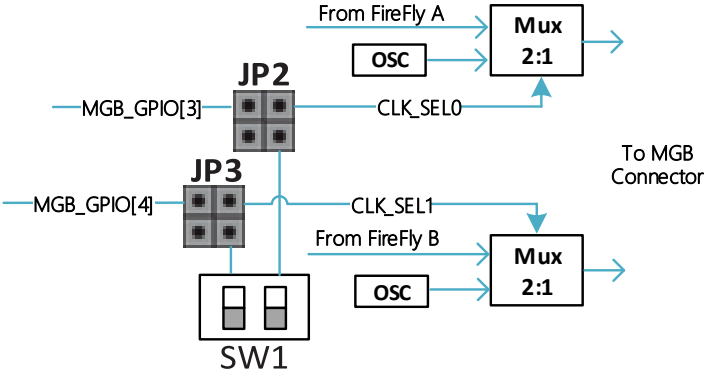


Figure 8: Switch select clock input

Tables 1 list various ways of connecting the control signals using jumper headers available on the FIREFLY_MGB card

Control Pin	Jumper	Source Configuration		
LED1	JP1	Pin 1-2: MGBIO[5] when JP1 pin 1-2		
LED2	JP1	Pin 3-4: MGBIO[6] when JP1 pin 3-4		
CLK_SEL0	JP2	Pin 1-2: MGBIO[3] when JP2 pin 1-2		
		Pin 2-4: SW1	on	External DIFF clock input (FIREFLY A)
			off	oscillator
CLK_SEL1	JP3	Pin 1-2: MGBIO[4] when JP3 pin 1-2		
		Pin 2-4: SW1	on	External DIFF clock input (FIREFLY B)
			off	oscillator
I2C_SW_RSTN	JP4	MGBIO[9] when JP4 pin 1-2		
GPIO_RSTN	JP4	MGBIO[10] when JP4 pin 3-4		

Table 1: FIREFLY_MGB Control Signals

I2C BUS SWITCH and GPIO Expanders

I2C BUS SWITCH

I2C BUS SWITCH is an octal bi-directional translating switch controlled by the I2C bus.

The I2C upstream pair fans out to eight downstream pairs.

Any individual channel can be selected, determined by the contents of the programmable Control Register. For additional information on the NXP PCA9548 8-channel I2C switch, refer to the PCA9548 data sheet on the http://www.nxp.com website.

Pin	Function	Note
SCL	MGB_CPIO7	I2C BUS SWITCH upstream pair
SDA	MGB_CPIO8	
SD0	Si570_1_SDA	Downstream pair. The control interface to the Si570.
SC0	Si570_1_SCL	
SD1	Si570_2_SDA	Downstream pair. The control interface to the Si570.
SC1	Si570_2_SCL	
SD2	FF_SDA1	Downstream pair. The control interface to the FireFly connector.
SC2	FF_SCL1	
SD3	FF_SDA2	Downstream pair. The control interface to the FireFly connector.
SC3	FF_SCL2	
SD4	GPIO_EXPANDER_SDA	Downstream pair. The control interface to the GPIO Expander.
SC4	GPIO_EXPANDER_SCL	

Table 3: I2C BUS SWITCH I/O Pins

GPIO Expanders

There are two GPIO expanders available for providing additional I/O capability. The GPIO expanders are accessed and controlled through SCL and SDA as shown in Figure 4, on page 10.

For additional information on the NXP PCA9557 I/O expander and how to access the I/O ports, refer to the PCA9557 data sheet on the http://www.nxp.com website.

The I2C hex addresses for accessing the on-board I/O expanders are set to:

GPIO Expander A (GEA): 0x18
GPIO Expander B (GEB): 0x1C

Pin	Function	Note
IO0	FF_MODPRS1	The control signals to the FireFly connector
IO1	FF_MODPRS2	
IO2	FF_INT1	
IO3	FF_INT2	
IO4	TP7	
IO5	TP8	
IO6	TP9	
IO7	TP10	

Table 4: GPIO Expander A I/O Pins

Pin	Function	Note
IO0	FF_RESET1	The control signals to the FireFly connector
IO1	FF_RESET2	
IO2	FF_MODSEL1	
IO3	FF_ MODSEL 2	
IO4	LED1	GPIO pin and LED for user-specific application
IO5	LED2	
IO6	LED3	
IO7	LED4	

Table 5: GPIO Expander B I/O Pins

LEDs

There are four LEDs on the FIREFLY_MGB. User-defined LEDs can be configured through GPIO expanders to use them according to specific user cases. Some LED inputs are shared with general use I/0s, see Figure 4, on page 10.

LED	Function
LED1	Activity LED by MGBIO[5] when JP1 pin 1-2 or User defined
LED2	Activity LED by MGBIO[6] when JP1 pin 3-4 or User defined
LED3	User defined
LED4	User defined

Table 6: LED Configuration Table

FIREFLY_MGB Pin Tables

Table 7: MGB Connector J1 to QSFP+ Sockets J2A/J2B

FireFly Pin and connector		Name	MGB J1 Pin		Name	FireFly Pin and connector	
		3.3V	1	2	3.3V		
		GND	3	4	GND		
	A3	TXP[0]	5	6	RXP[0]	B17	
	A2	TXN[0]	7	8	RXN[0]	B18	
		GND	9	10	GND		
	B2	TXN[1]	11	12	RXN[1]	A17	
	B3	TXP[1]	13	14	RXP[1]	A18	
		GND	15	16	GND		
	-	REFCLKP[1]	17	18	REFCLKP[0]		
	-	REFCLKN[1]	19	20	REFCLKN[0]		J2
		GND	21	22	GND		
J2	A6	TXP[2]	23	24	RXP[2]	B14	
	A5	TXN[2]	25	26	RXN[2]	B15	
		GND	27	28	GND		
	B6	TXN[3]	29	30	RXN[3]	A15	
	B5	TXP[3]	31	32	RXP[3]	A14	
		GND	33	34	GND		
	A12	MGBIO[1]	35	36	MGBIO[6]	A11	
	A11	MGBIO[2]	37	38	MGBIO[7]		
	B12	MGBIO[3]	39	40	MGBIO[8]		
	B11	MGBIO[4]	41	42	MGBIO[9]	B12	
	A12	MGBIO[5]	43	44	MGBIO[10]	B11	
		GND	45	46	GND		
	A3	TXP[4]	47	48	RXP[4]	B17	
	A2	TXN[4]	49	50	RXN[4]	B18	
		GND	51	52	GND		
	B2	TXN[5]	53	54	RXN[5]	A17	
	B3	TXP[5]	55	56	RXP[5]	A18	
		GND	57	58	GND		J3
J3	-	REFCLKP[3]	59	60	REFCLKP[2]		
	-	REFCLKN[3]	61	62	REFCLKN[2]		
		GND	63	64	GND		
	A6	TXP[6]	65	66	RXP[6]	B14	
	A5	TXN[6]	67	68	RXN[6]	B15	
		GND	69	70	GND		
	B6	TXN[7]	71	72	RXN[7]	A15	
	B5	TXP[7]	73	74	RXP[7]	A14	
		GND	75	76	GND		
		SCK	77	78	A0		
		SDA	79	80	A1		

Table 8: FireFly Connector J2/J3 to MGB Connector J1

Connector J2		MGB J1
Pin	Trace Name	Pin
A1	GND	
A2	TXA_N0	7
A3	TXA_P0	5
A4	GND	
A5	TXA_N2	25
A6	TXA_P2	23
A7	GND	
A8	CLK2MGB_P0	
A9	CLK2MGB_N0	
A10	GND	
A11	MGB_GPIO2	37
A12	MGB_GPIO1	35
A13	GND	
A14	RXA_P3	32
A15	RXA_N3	30
A16	GND	
A17	RXA_P1	14
A18	RXA_N1	12
A19	GND	
B1	GND	
B2	TXA_N1	11
B3	TXA_P1	13
B4	GND	
B5	TXA_N3	29
B6	TXA_P3	31
B7	GND	
B8	-	
B9	-	
B10	GND	
B11	MGB_GPIO4	41
B12	MGB_GPIO3	39
B13	GND	
B14	RXA_P2	24
B15	RXA_N2	26
B16	GND	
B17	RXA_P0	6
B18	RXA_N0	8
B19	GND	

Connector J3		MGB J1
Pin	Trace Name	Pin
A1	GND	
A2	TXB_N0	49
A3	TXB_P0	47
A4	GND	
A5	TXB_N2	67
A6	TXB_P2	65
A7	GND	
A8	CLK2MGB_P1	
A9	CLK2MGB_N1	
A10	GND	
A11	MGB_GPIO6	36
A12	MGB_GPIO5	43
A13	GND	
A14	RXB_P3	74
A15	RXB_N3	72
A16	GND	
A17	RXB_P1	56
A18	RXB_N1	54
A19	GND	
B1	GND	
B2	TXB_N1	55
B3	TXB_P1	53
B4	GND	
B5	TXB_N3	73
B6	TXB_P3	71
B7	GND	
B8	-	
B9	-	
B10	GND	
B11	MGB_GPIO10	44
B12	MGB_GPIO9	42
B13	GND	
B14	RXB_P2	66
B15	RXB_N2	68
B16	GND	
B17	RXB_P0	48
B18	RXB_N0	50
B19	GND	

Table 9: MGB I/O Interface

MGB I/O Assignments			
I/O	**Connector**	**Signal**	
MGBIO[1]	J2	MGB_GPIO1	
MGBIO[2]		MGB_GPIO2	
MGBIO[3]	JP2,J2	JP2	CLK_SEL0
		J2	MGB_GPIO3
MGBIO[4]	JP2,J2	JP2	CLK_SEL1
		J2	MGB_GPIO4
MGBIO[5]	JP1,J3	JP1	LED D1
		J3	MGB_GPIO5
MGBIO[6]		JP1	LED D2
		J3	MGB_GPIO6
MGBIO[7]	U11	I2C_SCL	
MGBIO[8]		I2C_SDA	
MGBIO[9]	JP4,J3	JP4	I2C_SW_RSTN
		J3	MGB_GPIO9
MGBIO[10]		JP4	GPIO_RSTN
		J3	MGB_GPIO10

Table 10: FireFly Connector J4/J5 to GPIO Expander A

FireFly Connector	GPIO Expander A I/Os	
J4	0	FF_MODPRS1
	2	FF_INT1
J5	1	FF_MODPRS2
	3	FF_INT2
	4	TP7
	5	TP8
	6	TP9
	7	TP10

Table 11: FireFly Connector J4/J5 to GPIO Expander B

FireFly Connector	GPIO Expander B I/Os	
J4	0	FF_ RESET 1
	2	FF_MODSEL1
J5	1	FF_ RESET2
	3	FF_MODSEL2
	4	LED1
	5	LED2
	6	LED3
	7	LED4

Table 12: MGB Pin Table

Trace Name	J1 Pin		Trace Name
3.3V	1	2	3.3V
GND	3	4	GND
TXP[0]	5	6	RXP[0]
TXN[0]	7	8	RXN[0]
GND	9	10	GND
TXN[1]	11	12	RXN[1]
TXP[1]	13	14	RXP[1]
GND	15	16	GND
REFCLKP[1]	17	18	REFCLKP[0]
REFCLKN[1]	19	20	REFCLKN[0]
GND	21	22	GND
TXP[2]	23	24	RXP[2]
TXN[2]	25	26	RXN[2]
GND	27	28	GND
TXN[3]	29	30	RXN[3]
TXP[3]	31	32	RXP[3]
GND	33	34	GND
MGBIO[1]	35	36	MGBIO[6]
MGBIO[2]	37	38	MGBIO[7]
MGBIO[3]	39	40	MGBIO[8]
MGBIO[4]	41	42	MGBIO[9]
MGBIO[5]	43	44	MGBIO[10]
GND	45	46	GND
TXP[4]	47	48	RXP[4]
TXN[4]	49	50	RXN[4]
GND	51	52	GND
TXN[5]	53	54	RXN[5]
TXP[5]	55	56	RXP[5]
GND	57	58	GND
REFCLKP[3]	59	60	REFCLKP[2]
REFCLKN[3]	61	62	REFCLKN[2]
GND	63	64	GND
TXP[6]	65	66	RXP[6]
TXN[6]	67	68	RXN[6]
GND	69	70	GND
TXN[7]	71	72	RXN[7]
TXP[7]	73	74	RXP[7]
GND	75	76	GND
SCK	77	78	A0
SDA	79	80	A1