HDMI_HT3
EH1706003017
Reference Manual

March 2018 ver0.1

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Revision History

Date	Rev	Comment
Mar 2018	v0	Initial version
Nov 2018	v1	HDMI Pin

Contents

IMPORTANT!

ESD

The HAPS®SOC_NORF_HT3 Transceiver Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

•Transport the card in an ESD bag

•Wear an anti-static wrist strap

•Make sure the work area is equipped with an ESD mat

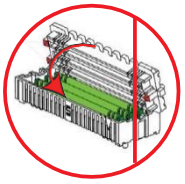
Warning

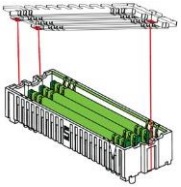
Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

HapsTrak® 3 Connector Considerations

The HT3 connectors must be attached carefully! If connected improperly socket pins can be deformed or holding rail ends can become damaged.

When connecting daughter boards and HT3 cable connectors, they should be held parallel to the SOC_NORF_HT3 connector throughout the mating process.





Overview

This document is the HDMI_HT3 Reference Manual and describes the functions of the HDMI_HT3 daughter board.

The HDMI_HT3 daughter board may be set up for configure HDMI Transmitter through HT3. Offer input data for HDMI video out.

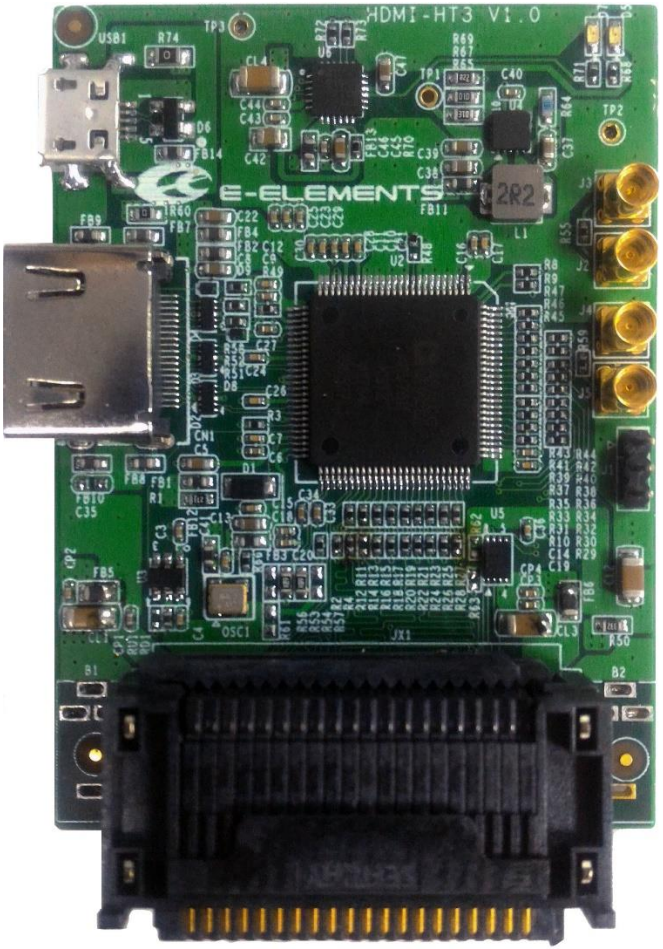


Figure 1: Top View of HDMI_HT3

HDMI_HT3 daughter board consists of:

- 1 HT3 Connector, Power
- 1 HDMI 1.4 Connector
- 1 USB-Micro-B Connector
- 2 pairs of Differential MMCX Clock Connectors (for Global Clocks)

Layout

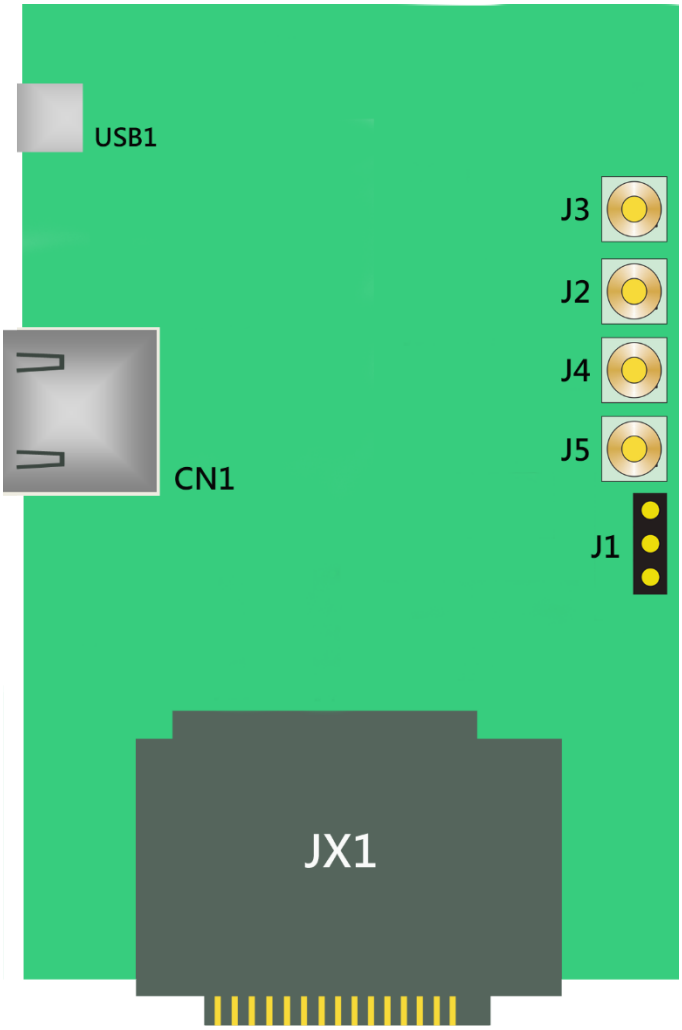


Figure 2: HDMI_HT3 Layout

Block Diagram

Figures 3 show the connectivity between the HDMI_HT3 daughter board's HDMI connector and connectors to the HT3 connector. The HT3 I/O pin mapping is described in the JX1 pin table on page 13.

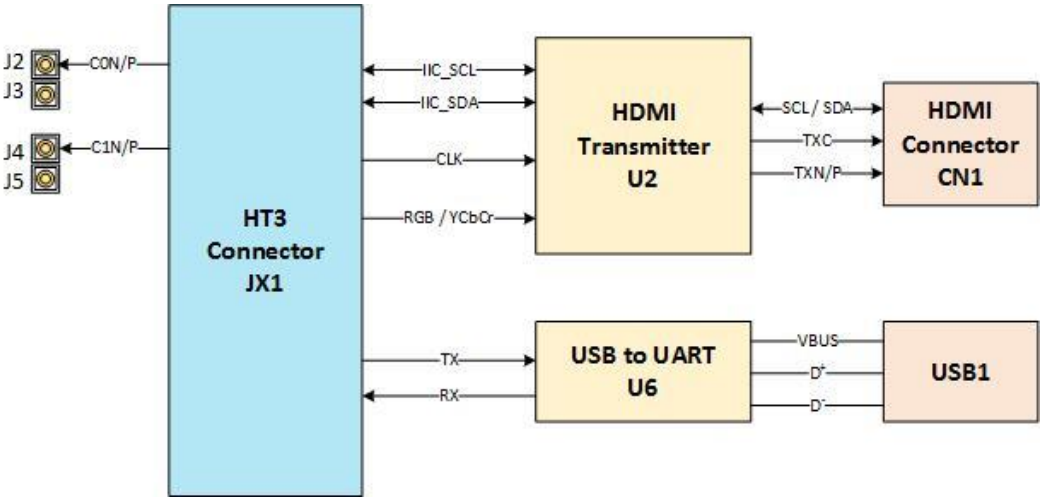


Figure 3: HDMI_HT3 Block Diagram

Card Placement

HAPS-80

HAPS-80 systems include 24 HT3 Connector for each FPGA. The HapsTrak 3 (HT3) is a 160-pin connector containing 52 signal pins, most of which can be used for single ended or differential signaling. All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

The HDMI_HT3 daughter board may be set up by HT3. Figure 4 shows an example setup with a HAPS-80 system.

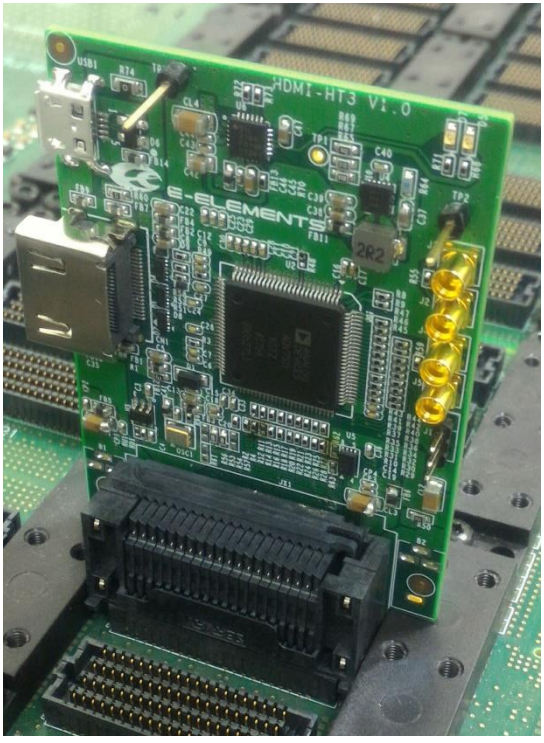


Figure 4: HDMI_HT3 mounted on HAPS-80 system

HDMI Transmitter

The ADV7511 is a 225 MHz High-Definition Multimedia Interface transmitter located at U2. Supports the HDMI 1.4-specific features, HEAC (ARC), and 3D video. allows the secure transmission of protected content as specified by the HDCP 1.4 protocol.

The ADV7511 accepts video data from as few as eight pins (either YCbCr 4:2:2 double data rate [DDR] or YCbCr 4:2:2 with 2x pixel clock) or as many as 36 pins (RGB 4:4:4 or YCbCr 4:4:4). In addition it accepts HSYNC, VSYNC and DE (Data Enable).

Mode	Format	Input Data D[35:0]																																	
		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
36	RGB	R[11:0]												G[11:0]												B[11:0]											
bit	YCrCb	Cr[11:0]												Y[11:0]												Cb[11:0]											
30	RGB	R[9:0]												G[9:0]												B[9:0]											
bit	YCrCb	Cr[9:0]												Y[9:0]												Cb[9:0]											
24	RGB	R[7:0]												G[7:0]												B[7:0]											
bit	YCrCb	Cr[7:0]												Y[7:0]												Cb[7:0]											
Pins D[35:0]		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 1: Normal RGB or YCbCr 4:4:4 with Separate Syncs; Input ID = 0

Clocks

MMCX connectors for clock connection between the user FPGA and other components in a hardware setup.

MMCX Connector	Differential or Single- ended	Direction	Source or Destination	
J2/J3	DIFF	Output	Source	C0P/C0N
J4/J5	DIFF	Output		C1P/C1N

Table 2: MMCX Clock Connections

Output Clocks

Output clocks are internal signals (FPGA generated clocks or HAPS global clocks) that travel from the HAPS system through the HDMI_HT3 daughter board.

Access to the HAPS system's differential global clock (GCLK) signals are available through the Output clock SMB connector pairs on the HDMI_HT3 daughter board. Table 2 is a list of clock connections for each MMCX connector.

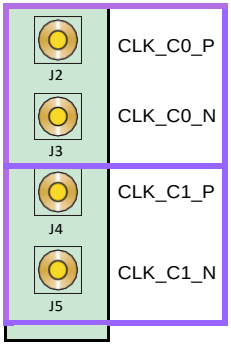


Figure 5: DIFF Clocks

Pin Tables

JX1

JX1 (A0-B13)					JX1 (C0-C1P)				
Pin	Trace Name	Connector			Pin	Trace Name	Connector		
A0	HDMI_INT	U2	VCCO		C0	HDMI_D14	U2	VCCO	
A1	IIC_SCL_HDMI				C1	HDMI_D13			
A2	HDMI_D31				C2	HDMI_D8			
A3	HDMI_D30				C3	HDMI_D7			
A4	IIC_SDA_HDMI				C4	HDMI_D12			
A5	HDMI_D35				C5	HDMI_D11			
A6	HDMI_D29				C6	HDMI_D6			
A7	HDMI_D28				C7	HDMI_D5			
A8	HDMI_D34				C8	HDMI_D10			
A9	HDMI_D33				C9	HDMI_D9			
A10	HDMI_D27				C10	HDMI_D4			
A11	HDMI_D26				C11	HDMI_D3			
A12					C12				
A13					C13				
B0	HDMI_D25	U2	VCCO		D0	HDMI_D2	U2	VCCO	
B1	HDMI_D24				D1	HDMI_D1			
B2	HDMI_D19				D2	USB_UART_TX	U6	VCCO	
B3	HDMI_D18				D3	USB_UART_RX			
B4	HDMI_D23				D4	HDMI_D0	U2	VCCO	
B5	HDMI_D22				D5	HDMI_DE			
B6	HDMI_D17				D6	JX1_D6	J1	VCCO	
B7	HDMI_CLK				D7	HDMI_D32	D4	3.3V	
B8	HDMI_D21				D8	HDMI_HSYNC			
B9	HDMI_D20				D9	HDMI_VSYNC			
B10	HDMI_D16				D10	HDMI_SPDIF			
B11	HDMI_D15				D11	HDMI_SPDIF_OUT_LS			
B12					D12				
B13					D13				
					C0N	CLK_C0_N	J2	VCCO	DIFF
	U2 HDMI				C0P	CLK_C0_P	J3	VCCO	
	U6 UART				C1N	CLK_C1_N	J4	VCCO	
	J1 GPIO				C1P	CLK_C1_P	J5	VCCO	
	J2/J3/J4/J5 Differential Clock								