SDIO_EMMC5.1_HT3
EH2019002035
Reference Manual

June 2021 ver0.4

Copyright Notice and Proprietary Information

Third-Party Links

Any links to third-party websites included in this document are for your convenience only. E-elements does not endorse and is not responsible for such websites and their practices, including privacy practices, availability, and content.

E-ELEMENTS TECHNOLOGY CO., LTD.

5F, No.61, Lane76, RuiguangRd.,

Neihu Dist., Taipei,

Taiwan, R.O.C.

www.e-elements.com

Revision History

Date	Rev	Comment
Nov 2020	V0.1	Initial version.
Mar 2021	V0.2	Add DS pin of EMMC
Mar 2021	V0.3	Add level shift to SD I/O.
Jun 2021	V0.4	Correct the SD3.0 to SD2.0 and the block diagram

Contents

SDIO_EMMC5.1_HT3

IMPORTANT!

ESD

The SDIO_EMMC5.1_HT3 Transceiver Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

•Transport the card in an ESD bag

•Wear an anti-static wrist strap

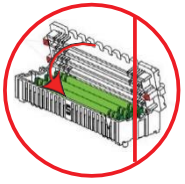
•Make sure the work area is equipped with an ESD mat

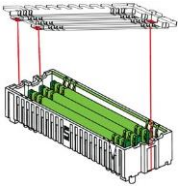
Warning

Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS® system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

HapsTrak® 3 Connector Considerations

The HT3 connectors must be attached carefully! If connected improperly socket pins can be deformed or holding rail ends can become damaged.





Overview

This document is the SDIO_EMMC5.1_HT3 Reference Manual and describes the functions of the SDIO_EMMC5.1_HT3 daughter board.

The SDIO_EMMC5.1_HT3 daughter board includes one micro-USB connector providing four RS-232 connection through a standard USB cable, connectivity for 20-pin ARM Cortex Debug interface, 10-pin GPIO connector and SD2.0 Socket.

The SDIO_EMMC5.1_HT3 daughter board also includes onboard memory. One 32Gb EMMC memory and one 256Mb QSPI memory.

Figure 1: Top View of SDIO_EMMC5.1_HT3 daughter board

Layout

SDIO_EMMC5.1_HT3 daughter board consists of:

- 1 20-pin ARM Cortex Debug + ETM Connector
- 1 Micro-USB Ports
- 1 SD2.0 Socket
- 1 EMMC Memory
- 1 QSPI Memory
- 1 10-pin GPIO connector

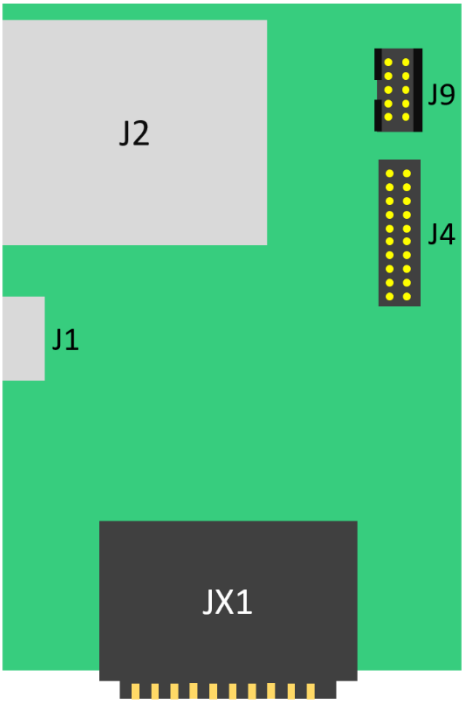


Figure 2: Top of SDIO_EMMC5.1_HT3 board layout

Block Diagram

Figure 4 show the connectivity between the SDIO_EMMC5.1_HT3 daughter board's headers and connectors to the HT3 connector. The HT3 I/O pin mapping is described in the JX1 pin table on page 13.

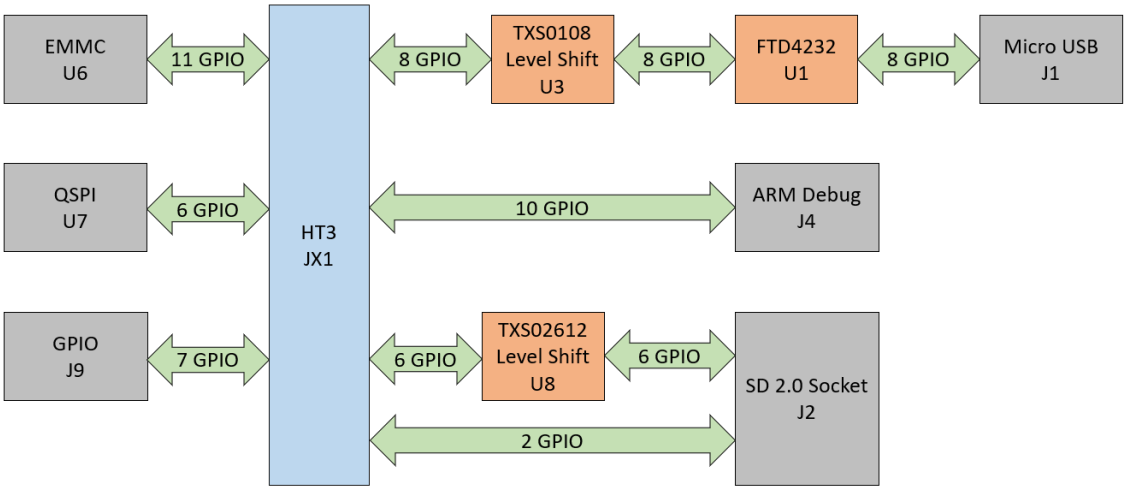


Figure 3: SDIO_EMMC5.1_HT3 Block Diagram

Daughter Board Placement

HAPS-80 systems include 24 HT3 Connector for each FPGA. The HapsTrak 3 (HT3) is a 160-pin connector containing 52 signal pins, most of which can be used for single ended or differential signaling. All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

The SDIO_EMMC5.1_HT3 card connected to HAPS-80 through HT3 connector, Figure 5 is the example of card installed.

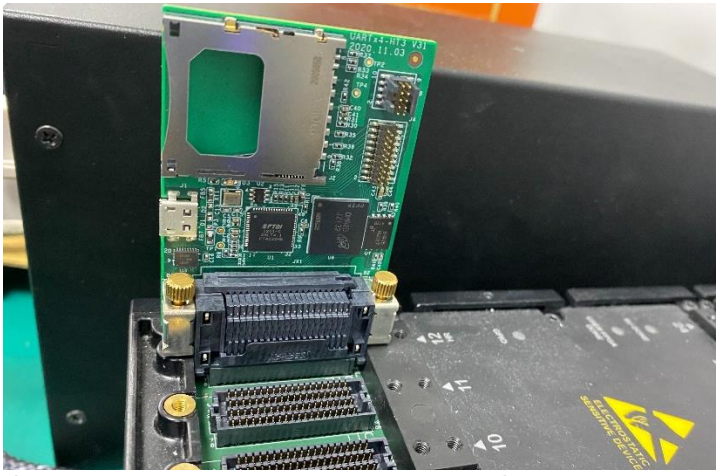


Figure 4: SDIO_EMMC5.1_HT3 mounted on HAPS-80 system

ARM Debug Interface

SDIO_EMMC5.1_HT3 provides connectivity between connector J4 to user FPGA I/O pins through the HT3 connector. J4 is a 20-pin header with ground and signals arranged for ARM debug interface. Connect the proper signals in the user FPGA design from the FPGA internal ARM core debug ports to the HT3 pins according to the pin mapping depicted in the JX1 pin table on page 13. The ten I/Os allocated to this interface are routed to the ARM connector from GPIO Header JX1 and are also available for alternate uses.

SD2.0 Card Socket

The SDIO_EMMC5.1_HT3 includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose nonvolatile SDIO memory cards and peripherals.

QSPI Memory

SDIO_EMMC5.1_HT3 includes an on-board SPI memory (U7, MT25QU256ABA1EW9, 256Mb) to provide a storage solution for your design. Pin locations on FPGA are list below.

U7		JX1
Pin	Trace Name	Pin
1	QSPI_CS_N	D11
2	QSPI_D1	C9
3	QSPI_D2	C10
4	GND	-
5	QSPI_D0	C5
6	QSPI_CLK	C8
7	QSPI_D2	C11
8	1.8V	-

EMMC Memory

SDIO_EMMC5.1_HT3 includes an on-board EMMC memory (U6, MTFC32GAPALBH, 32Gb) to provide a storage solution for your design. Pin locations on FPGA are list below.

U6		JX1
Pin	Trace Name	Pin
D0	EMMC0_D0	B0
D1	EMMC0_D1	B1
D2	EMMC0_D2	B2
D3	EMMC0_D3	B3
D4	EMMC0_D4	B4
D5	EMMC0_D5	B5
D6	EMMC0_D6	B6
D7	EMMC0_D7	B7
RST#	EMMC0_RESET_N	A1
CMD	EMMC0_CMD	A0
CLK	EMMC0_CLK	B8
DS	EMMC0_DS	B9

Micro-USB Port

The micro-USB connector provides four RS-232 connection through a standard USB cable to your host computer. Designs that utilize an UART module may connect to the USB/UART pins to be accessed and controlled through a terminal application.

FTDI FX4232HL is used to bridge UART and USB. Download and install the Virtual COM port (VCP) driver from ftdichip.com. The driver allows the USB device to appear as a COM port available to the host computer. Application software can access the USB device in the same way as it would access a standard COM port.

Part: USB to serial UART Interface
Number: FT4232HL
Web address: ftdichip.com

Note: VCCO must be configured to 1.8V

Pin Tables

HT3 Connector

JX1									
(A0-B13)					(C0-D13)				
Pin	Trace Name	Connector			Pin	Trace Name	Connector		
A0	EMMC0_CMD	U6	VCCO		C0	UART_TXD2	J1	VCCO	
A1	EMMC0_RESET_N				C1	UART_TXD0			
A2	SD_D0	J2	VCCO		C2	UART_RXD0			
A3	SD_D1				C3	UART_TXD3			
A4	SD_D2				C4	UART_RXD3			
A5	SD_D3				C5	QSPI_D0	U7	VCCO	
A6	SD_CLK				C6	UART_TXD1	J1	VCCO	
A7	SD_CD_N				C7	UART_RXD1			
A8	SD_CMD				C8	QSPI_CLK	U7	VCCO	
A9	SD_WP				C9	QSPI_D1			
A10	GPIO_A10	J9	VCCO		C10	QSPI_D2			
A11	GPIO_A11				C11	QSPI_D3			
A12	GPIO_A12				C12				
A13					C13				
B0	EMMC0_D0	U6	VCCO		D0	UART_RXD2	J1	VCCO	
B1	EMMC0_D1				D1	TMS_SWDIO	J4	VCCO	
B2	EMMC0_D2				D2	TCK_SWDCLK			
B3	EMMC0_D3				D3	TDO_SWO			
B4	EMMC0_D4				D4	TDI_NC			
B5	EMMC0_D5				D5	ARM_RESER_N			
B6	EMMC0_D6				D6	TRACE_CLK			
B7	EMMC0_D7				D7	TRACE_D0			
B8	EMMC0_CLK				D8	TRACE_D1			
B9	EMMC0_DS				D9	TRACE_D2			
B10	GPIO_B10	J9	VCCO		D10	TRACE_D3			
B11	GPIO_B11				D11	QSPI_CS_N	U7	VCCO	
B12					D12	GPIO_D12	J9	VCCO	
B13					D13				

	J1 UART
	U6 EMMC
	J2 SD
	J9 GPIO
	U7 QSPI
	J4 ARM Debug

ARM Cortex Debug+ETM Connector

J4(Stacked board)				JX1
Trace Name	Pin	Pin	Trace Name	Pin
VCCO	1	2	TMS_SDWIO	D1
GND	3	4	TCK _SWDCLK	D2
	5	6	TDO_ SWD	D3
	7	8	TDI _NC	D4
	9	10	ARM_RESET_N	D5
	11	12	TRACE_CLK	D6
	13	14	TRACE_D0	D7
	15	16	TRACE_D1	D8
	17	18	TRACE_D2	D9
	19	20	TRACE_D3	D10

GPIO

JX1	J9				JX1
Pin	Trace Name	Pin	Pin	Trace Name	Pin
-	VCCO	1	2	-	
A10	GPIO_A10	3	4	GPIO_B10	B10
A11	GPIO_A11	5	6	GPIO_B11	B11
A12	GPIO_A12	7	8	GPIO_D12	D12
-	GND	9	10	-	

SD2.0 Socket

J2		JX1
Pin	Trace Name	Pin
1	SD_D3	A5
2	SD_CMD	A8
3	GND	-
4	3.3V	-
5	SD_CLK	A6
6	GND	-
7	SD_D0	A2
8	SD_D1	A3
9	SD_D2	A4
10	SD_CD_N	A7
11	SD_WP	A9
12	-	