SFP28_HT3
Reference Manual

July 2019 ver1.1

E-ELEMENTS

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Revision History

Date	Rev	Comment
Oct. 2018	v0	Initial version
Jul 2019	v1	Add jumpers to select powered by external power or HT3 power

Contents

IMPORTANT!

ESD:

The SFP28_HT3 Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

- Transport the card in an ESD bag
- Wear an anti-static wrist strap
- Make sure the work area is equipped with an ESD mat

Warning

Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS® system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

Overview

This document is the SFP28_HT3 Reference Manual and describes the functions of the SFP28_HT3 interface card.

The SFP28_HT3 daughter board includes FireFly transceiver connectors that support up to high-speed serial links over three FireFly cables.

The SFP28_HT3 daughter board includes SFP28, SFP28 is a 25 Gbit/s interface which has evolved from 100 Gigabit Ethernet, which is typically implemented with 4 × 25 Gbit/s data lanes.

Figure 1: Top View of SFP28_HT3

Layout

SFP28_HT3 daughter board consists of:

- 1 12-pin PMOD Connector
- 2 pairs of Differential MMCX Clock Connectors (for Global Clocks)
- 1 SFP28
- 1 FIREFLY Connectors
- 1 HT3 Connectors

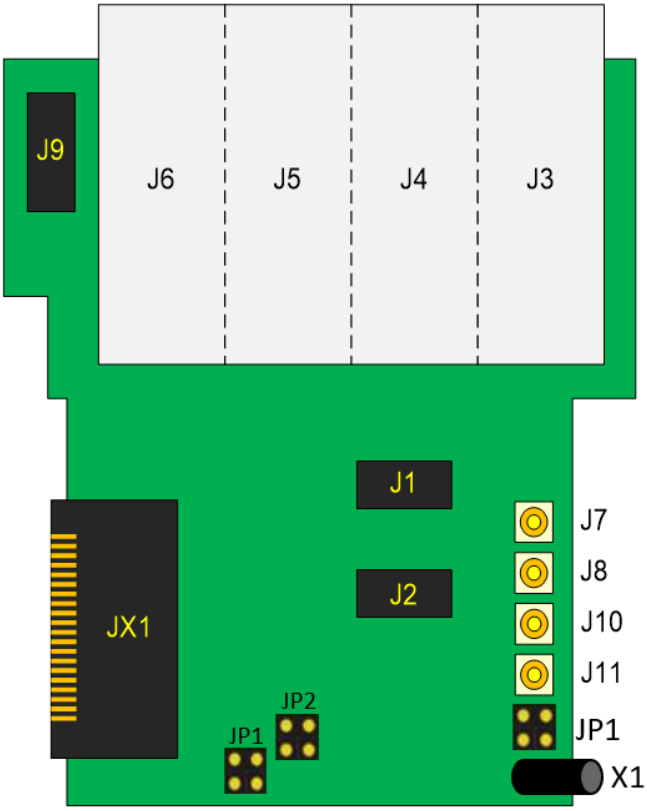

Figure 2: Top SFP28_HT3 Card Layout

Block Diagram

Figure 3 shows the connectivity between the SFP28_HT3 daughter board's headers and connectors to the HT3 connector. The HT3 I/O pin mapping is described in the JX1 pin table on page 16.

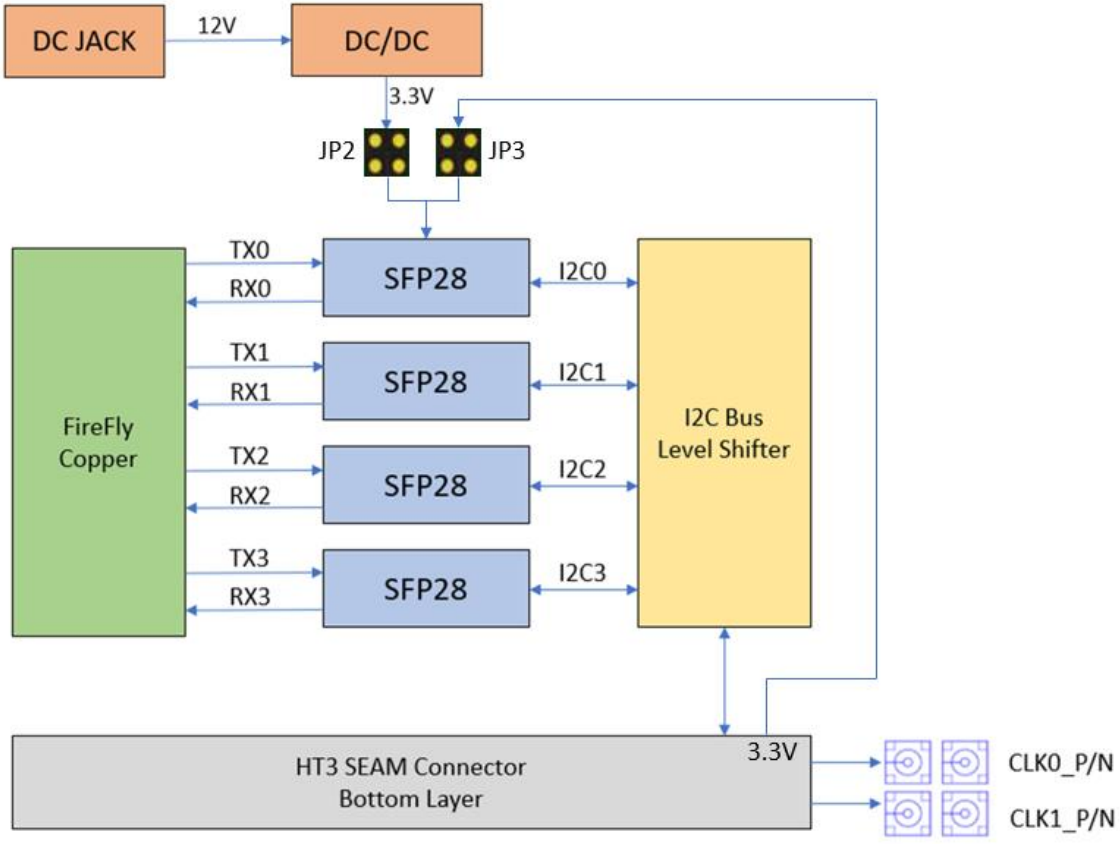

Figure 3: SFP28_HT3 Architecture Block Diagram

Card Placement

HAPS-80

HAPS-80 systems include 24 HT3 Connector for each FPGA. The Haps Trak 3 (HT3) is a 160-pin connector containing 52 signal pins, most of which can be used for single-ended or differential signaling. All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

The SFP28_HT3 card connected to HAPS-80 through HT3 connector, Figure 4 is an example of card installed.

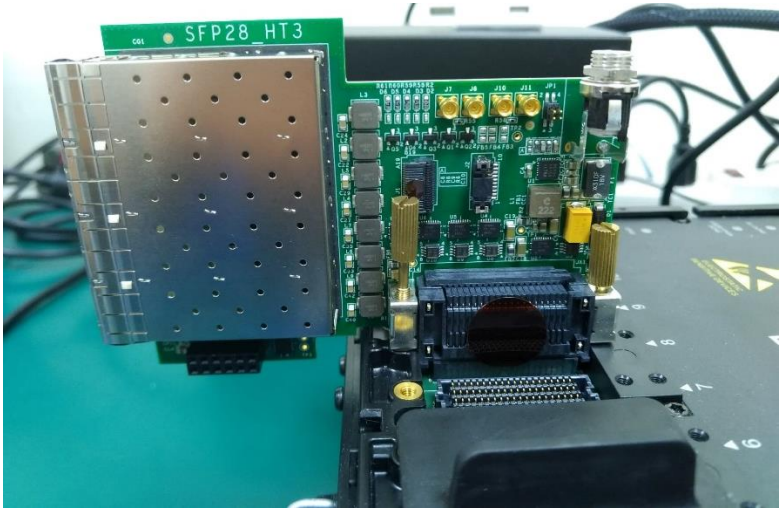

Figure 4: A SFP28 Interface Card Installed on a HAPS-80

Clocks

MMCX connectors for clock connections between the user FPGA and other components in a hardware setup.

Output Clocks

Output clocks are internal signals (FPGA generated clocks or HAPS global clocks) that travel from the HAPS system through the SFP28_HT3 daughter board.

Access to the HAPS system's differential global clock (GCLK) signals are available through the Output clock SMB connector pairs on the SFP28_HT3 daughter board. Table 1 is a list of clock connections for each MMCX connector.

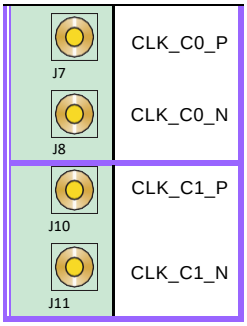

Figure 5: DIFF Clocks

MMCX Connector		Direction	Source
J7/J8	Differential	Output	C0P/C0N
J10/J11	Differential	Output	C1P/C1N

Table 1: MMCX Clock Connections

LEDs

There are five LEDs on the SFP28_HT3. User-defined LEDs can be configured through GPIO expanders to use them according to specific user cases.

LED	Function
D2	External 12V power led
D3	User defined(GPIO A12)
D4	User defined(GPIO D10)
D5	User defined(GPIO D11)
D6	User defined(GPIO D12)

Table 2: LED Configuration Table

Jumpers

Jumpers provide different configuration options dependent on the user requirements.

JPI configure the U1(LT8640S) power IC different operating mode. JP2 and JP3 configure the board powered either via HAPS80 HT3 connector or via an external power cable.

Jumper	Function
JP1	Pin 1-2: Burst mode Pin 3-4: Spread-Spectrum mode Open: Forced Continuous mode(default)
JP2	Pin1-2/Pin3-4: Powered by external power
JP3	Pin1-2/Pin3-4: Powered by HAPS80 HT3 connector(default)

Table 3: Jumper Configuration Table

SFP28

SFP28 is a 25 Gbit/s interface which has evolved from 100 Gigabit Ethernet, which is typically implemented with 4 × 25 Gbit/s data lanes. Identical in mechanical dimensions to SFP and SFP+, SFP28 implements one 28 Gbit/s lane[18] (25 Gbit/s + error correction) for top-of-rack switch to server connectivity.

SFP28 can be configured through GPIO to use them.

Configure Pin	Connect
SFP_TX_FAULT0	GPIO_A2
SFP_TX_DISABLE0	GPIO_A3
SFP_MOD_DEF0	GPIO_A4
SFP0_RS0	GPIO_A5
SFP_RX_LOS0	GPIO_A6
SFP0_RS1	GPIO_A7
SFP_SCL0	GPIO_A8
SFP_SDA0	GPIO_A9
SFP_TX_FAULT1	GPIO_B2
SFP_TX_DISABLE1	GPIO_B3
SFP_MOD_DEF1	GPIO_B4
SFP1_RS0	GPIO_B5
SFP_RX_LOS1	GPIO_B6
SFP1_RS1	GPIO_B7
SFP_SCL1	GPIO_B8
SFP_SDA1	GPIO_B9
SFP_TX_FAULT2	GPIO_C2
SFP_TX_DISABLE2	GPIO_C3
SFP_MOD_DEF2	GPIO_C4
SFP2_RS0	GPIO_C5
SFP_RX_LOS2	GPIO_C6
SFP2_RS1	GPIO_C7
SFP_SCL2	GPIO_C8
SFP_SDA2	GPIO_C9
SFP_TX_FAULT3	GPIO_D2
SFP_TX_DISABLE3	GPIO_D3
SFP_MOD_DEF3	GPIO_D4
SFP3_RS0	GPIO_D5
SFP_RX_LOS3	GPIO_D6
SFP3_RS1	GPIO_D7
SFP_SCL3	GPIO_D8
SFP_SDA3	GPIO_D9

FireFly Connector

Connector J1			
Pin	**Trace Name**	**Pin**	**Trace Name**
A1	GND	B1	GND
A2	SFP_RX_N0	B2	SFP_RX_N1
A3	SFP_RX_P0	B3	SFP_RX_P1
A4	GND	B4	GND
A5	SFP_RX_N2	B5	SFP_RX_N3
A6	SFP_RX_P2	B6	SFP_RX_P3
A7	GND	B7	GND
A8	-	B8	-
A9	-	B9	-
A10	GND	B10	GND
A11	-	B11	-
A12	-	B12	-
A13	GND	B13	GND
A14	SFP_TX_P3	B14	SFP_TX_P2
A15	SFP_TX_N3	B15	SFP_TX_N2
A16	GND	B16	GND
A17	SFP_TX_P1	B17	SFP_TX_P0
A18	SFP_TX_N1	B18	SFP_TX_N0
A19	GND	B19	GND

HT3 Connector

JX1 (A0-B13)					JX1 (C0-C1P)				
Pin	Trace Name	Connector			Pin	Trace Name	Connector		
A0	PMOD_PIN1	J9	3.3V		C0	PMOD_PIN5	J9	3.3V	
A1	PMOD_PIN2				C1	PMOD_PIN6			
A2	SFP_TX_FAULT0	J3	3.3V		C2	SFP_TX_FAULT2	J5	3.3V	
A3	SFP_TX_DISABLE0				C3	SFP_TX_DISABLE2			
A4	SFP_MOD_DEF0				C4	SFP_MOD_DEF2			
A5	SFP0_RS0				C5	SFP2_RS0			
A6	SFP_RX_LOS0				C6	SFP_RX_LOS2			
A7	SFP0_RS1				C7	SFP2_RS1			
A8	SFP_SCL0				C8	SFP_SCL0			
A9	SFP_SDA0				C9	SFP_SDA0			
A10	ECUO_PRESENTL	J2	3.3V		C10	ECUO_INTL	J2	3.3V	
A11	ECUO_SELECTL				C11	ECUO_RESETL			
A12	GPIO_A12	D3	3.3V		C12				
A13					C13				
B0	PMOD_PIN3	J9	3.3V		D0	PMOD_PIN7	J9	3.3V	
B1	PMOD_PIN4				D1	PMOD_PIN8			
B2	SFP_TX_FAULT1	J4	3.3V		D2	SFP_TX_FAULT3	J6	3.3V	
B3	SFP_TX_DISABLE1				D3	SFP_TX_DISABLE3			
B4	SFP_MOD_DEF1				D4	SFP_MOD_DEF3			
B5	SFP1_RS0				D5	SFP3_RS0			
B6	SFP_RX_LOS1				D6	SFP_RX_LOS3			
B7	SFP1_RS1				D7	SFP3_RS1			
B8	SFP_SCL0				D8	SFP_SCL0			
B9	SFP_SDA0				D9	SFP_SDA0			
B10	ECUO_SCL	J2	3.3V		D10	GPIO_D10	D4	3.3V	
B11	ECUO_SDA				D11	GPIO_D11	D5		
B12					D12	GPIO_D12	D6		
B13					D13				
					C0N	CLK_C0_N	J7	VCCO	DIFF
	J9 PMOD				C0P	CLK_C0_P	J8	VCCO	
	J3 / J4 / J5 / J6 SFP28				C1N	CLK_C1_N	J10	VCCO	
	D3 / D4 /D5 / D6…				C1P	CLK_C1_P	J11	VCCO	
	FireFly								

PMOD Connector

Board file trace name	U13 3.3V	J9 3.3V		U13 3.3V	Board file trace name
PMOD_IO[0]	GPIO_A0	1	2	GPIO_C0	PMOD_IO[4]
PMOD_IO[1]	GPIO_A1	3	4	GPIO_C1	PMOD_IO[5]
PMOD_IO[2]	GPIO_B0	5	6	GPIO_D0	PMOD_IO[6]
PMOD_IO[3]	GPIO_B1	7	8	GPIO_D1	PMOD_IO[7]
	GND	9	10	GND	
	3.3V	11	12	3.3V	