HAPS CONNECT MEMBER

SMF_HSIO_HT3
EH1901003027
Reference Manual

December 2020 v1.2

E-ELEMENTS

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Revision History

Date	Rev	Comment
Jul. 2019	v0	Initial version
Jul. 2019	v0.1	Add the HSIO bank voltage
Jul. 2019	v1	Add the SI570 clock information
Mar. 2020	v1.1	Add JX1, JX2, J4, J5, J6 and J7 FPGA Bank
Dec. 2020	v1.2	Add led, button and onboard clock bank voltage.

Contents

IMPORTANT!

ESD:

The SMF_HSIO_HT3 Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

- Transport the card in an ESD bag
- Wear an anti-static wrist strap
- Make sure the work area is equipped with an ESD mat

Warning

Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS® system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

Overview

This document is the SMF_HSIO_HT3 Reference Manual and describes the functions of the SMF_HSIO_HT3 interface card.

The SMF_HSIO_HT3 daughter board includes FIREFLY transceiver connectors that support up to high-speed serial links over three FIREFLY cables.

The SMF_HSIO_HT3 daughter board includes HSIO(High Speed IO) connector support to MIPI signal, connected with CSI and DSI daughter board.

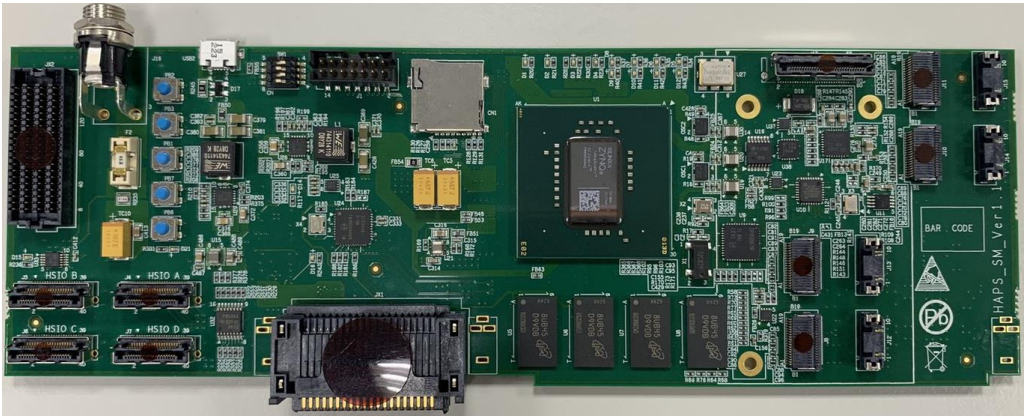

Figure 1: Top View of SMF_HSIO_HT3

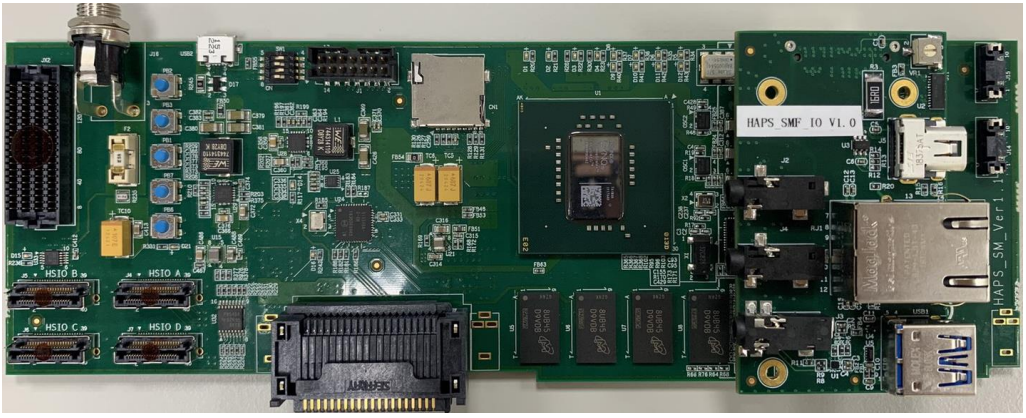

Figure 2: Top View of SMF_HSIO_HT3 with SMF_HSIO_HT3_IO

SMF_HSIO_HT3 daughter board consists of:

- 4 Firefly connectors
- 4 HSIO connectors
- 1 SD card Socket
- 1 mini DP connector (on SMF_HSIO_HT3_IO)
- 1 USB 2.0/3.0 connector (on SMF_HSIO_HT3_IO)
- 1 Ethernet connector (on SMF_HSIO_HT3_IO)
- 3 Audio connectors (on SMF_HSIO_HT3_IO)

Layout

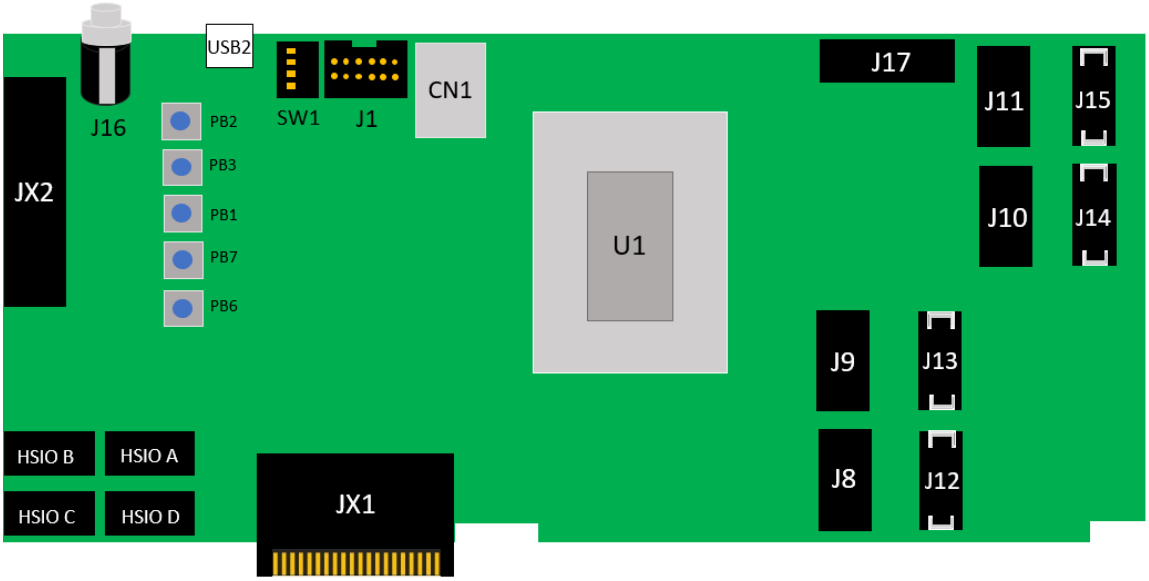

Figure 3: Top SMF_HSIO_HT3 Card Layout

Block Diagram

Figure 4 shows the connectivity of the SMF_HSIO_HT3 daughter board.

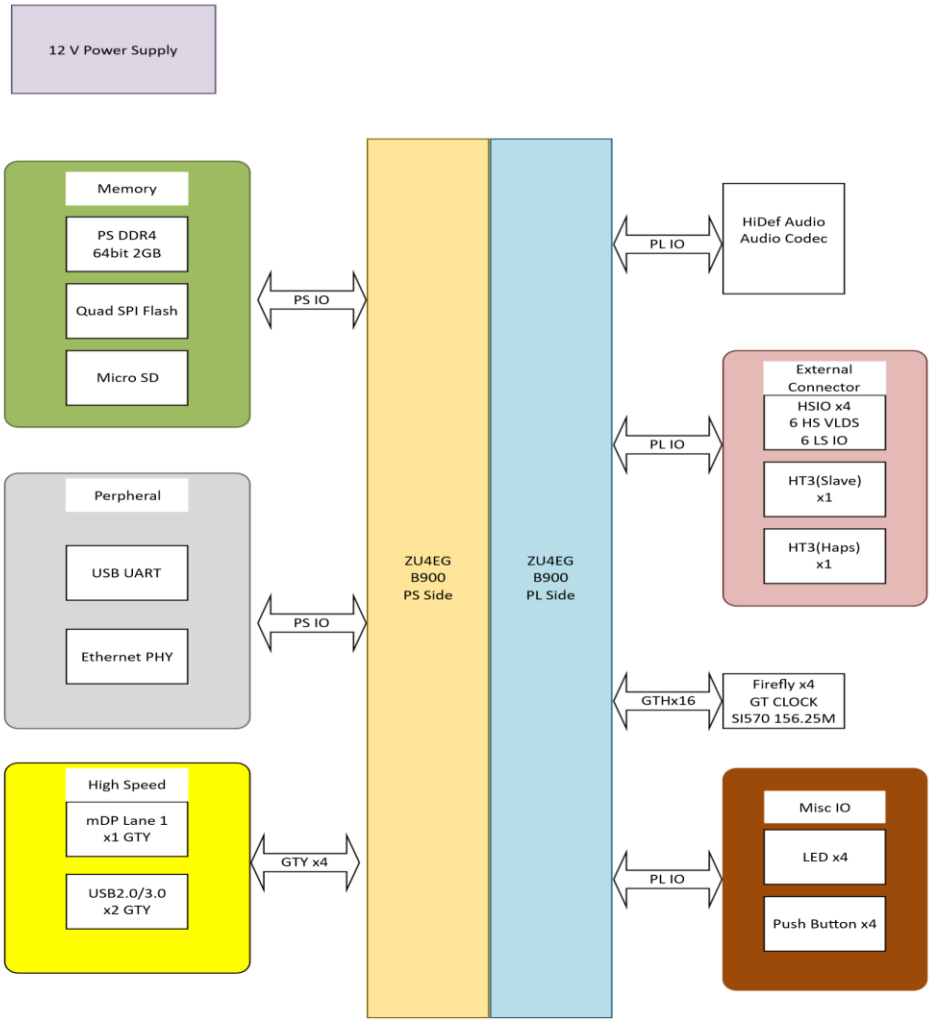

Figure 4: SMF_HSIO_HT3 Architecture Block Diagram

LEDs

There are sixteen led on the SMF_HSIO_HT3. User-defined LEDs can be configured to use them according to specific user cases.

LED	Function	Connected to	Bank Voltage
D1	PS_DONE		
D2	PS_INIT_B		
D3	PS_ERROR_OUT		
D4	PS_ERROR_STATUS		
D5	User defined	MIO20	1.8V
D6	User defined	MIO21	1.8V
D7	User defined	MIO22	1.8V
D8	User defined	MIO23	1.8V
D9	User defined	H16	1.8V
D10	User defined	J16	1.8V
D11	User defined	J14	1.8V
D12	User defined	J15	1.8V
D13	USB fault status		
D14	UART status		
D15	12V power		
D16	PS Reset status		

Button

There are five buttons on the SMF_HSIO_HT3. Two buttons can be used according to specific user cases.

LED	Function	Connected to	Bank Voltage
PB1	PS_PORG_B		
PB2	For users(default High)	MIO19	1.8V
PB3	For users(default High)	L15	1.8V
PB6	PS_POR_B		
PB7	PS_SRST_B		

Switch configures

SMF_HSIO_HT3 supports three config mode: JTAG、QSPI and microSD, using SW1 to switch between different configurations.

SMF_HSIO_HT3 has two 256Mb Flash chip, chip part number: MT25QU256ABA, it can be configured as an FPGA initialization

SMF_HSIO_HT3 also supports booting from microSD card, inserting a microSD card storing ZYNQ configuration image into SD card slot CN1.

Boot mode	Mode Pin[3:0]	SW1[1:4]
JTAG	0000	on-on-on-on
QSPI	0010	on-on-off-on
microSD	0101	on-off-on-off

Onboard CLK

SMF_HSIO_HT3 provides onboard clocks, for user to use.

Clock	Trace name	Frequency	Connected to U1 Pin	Bank Voltage
OSC2	FPGA_CLK_100MHZ	100MHz	G16	1.8V

PS MIO

HAPS_SMP provides 78 PS_MIO pins for versatile applications. Please refer to Zynq UltraScale+ MPSoC Technical Reference Manual (UG1085) for more PS_MIO information.

PS_MIO [0:25] Bank500	FPGA Pin	Trace Name	Type
MIO_0	H17	MIO0_QSPI0_SCLK	QSPI0
MIO_1	A20	MIO1_QSPI0_IO1	QSPI0
MIO_2	B19	MIO2_QSPI0_IO2	QSPI0
MIO_3	D19	MIO3_QSPI0_IO3	QSPI0
MIO_4	J17	MIO4_QSPI0_IO0	QSPI0
MIO_5	C19	MIO5_QSPI0_CS#	QSPI0
MIO_6	D20	Not Connected	NC
MIO_7	E19	MIO7_QSPI1_CS#	QSPI1
MIO_8	E20	MIO8_QSPI1_IO0	QSPI1
MIO_9	F20	MIO9_QSPI1_IO1	QSPI1
MIO_10	F18	MIO10_QSPI1_IO2	QSPI1
MIO_11	G18	MIO11_QSPI1_IO3	QSPI1
MIO_12	H18	MIO12_QSPI1_SCLK	QSPI1
MIO_13	G19	Not Connected	NC
MIO_14	E18	MIO14_I2C0_SCL	I2C0
MIO_15	J19	MIO15_I2C0_SDA	I2C0
MIO_16	K17	MIO16_I2C0_RST_N	I2C0
MIO_17	C18	MIO17_USB_RESET_N	USB
MIO_18	K18	MIO18_PHY_RESET_N	GEM3
MIO_19	K16	PS_BTN	GPIO
MIO_20	A19	MIO20_PS_LED0	GPIO
MIO_21	H19	MIO21_PS_LED1	GPIO
MIO_22	F17	MIO22_PS_LED2	GPIO
MIO_23	K19	MIO23_PS_LED3	GPIO
MIO_24	A18	Not Connected	NC
MIO_25	B18	MIO25_VBUS_DET	USB
PS_MIO [26:51] Bank501	**FPGA Pin**	**Trace Name**	**Type**
MIO_26	B20	MIO26_TLV320A_RSTn	NC
MIO_27	B21	MIO27_DP_AUX_OUT	DPAUX
MIO_28	A21	MIO28_DP_HPD	DPAUX
MIO_29	D21	MIO29_DP_OE	DPAUX
MIO_30	C21	MIO30_DP_AUX_IN	DPAUX
MIO_31	A22	MIO31_INA226_ALERT	POWER
MIO_32	G20	Not Connected	NC
MIO_33	C22	Not Connected	NC
MIO_34	B24	MIO34_UART0_RXD	UART0
MIO_35	B23	MIO35_UART0_TXD	UART0
MIO_36	D22	Not Connected	NC
MIO_37	F21	Not Connected	NC
MIO_38	C23	Not Connected	NC

MIO_39	E22	MIO39_SI5340A_RST_N	GPIO
MIO_40	C24	MIO40_SI5340A_OE_N	GPIO
MIO_41	D24	Not Connected	NC
MIO_42	E23	Not Connected	NC
MIO_43	F22	Not Connected	NC
MIO_44	E24	MIO44_SDIO_WP	SDIO
MIO_45	F23	MIO45_SDIO_CD	SDIO
MIO_46	K20	MIO46_SDIO_D0	SDIO
MIO_47	K21	MIO47_SDIO_D1	SDIO
MIO_48	J21	MIO48_SDIO_D2	SDIO
MIO_49	G21	MIO49_SDIO_D3	SDIO
MIO_50	J20	MIO50_SDIO_CMD	SDIO
MIO_51	H21	MIO51_SDIO_CLK	SDIO
PS_MIO [52:77] Bank502	**FPGA Pin**	**Trace Name**	**Type**
MIO_52	A24	MIO52_USB_CLK	USB
MIO_53	B25	MIO53_USB_DIR	USB
MIO_54	A23	MIO54_USB_D2	USB
MIO_55	B26	MIO55_USB_NXT	USB
MIO_56	A25	MIO56_USB_D0	USB
MIO_57	A26	MIO57_USB_D1	USB
MIO_58	A28	MIO58_USB_STP	USB
MIO_59	A27	MIO59_USB_D3	USB
MIO_60	C26	MIO60_USB_D4	USB
MIO_61	B29	MIO61_USB_D5	USB
MIO_62	B28	MIO62_USB_D6	USB
MIO_63	A29	MIO63_USB_D7	USB
MIO_64	B30	MIO64_PHY_TX_CLK	GEM3
MIO_65	D25	MIO65_PHY_TX_D0	GEM3
MIO_66	C27	MIO65_PHY_TX_D1	GEM3
MIO_67	C28	MIO65_PHY_TX_D2	GEM3
MIO_68	C29	MIO65_PHY_TX_D3	GEM3
MIO_69	D27	MIO69_PHY_TX_CTRL	GEM3
MIO_70	D26	MIO70_PHY_RX_CLK	GEM3
MIO_71	D30	MIO71_PHY_RX_D0	GEM3
MIO_72	E27	MIO71_PHY_RX_D1	GEM3
MIO_73	E30	MIO71_PHY_RX_D2	GEM3
MIO_74	E29	MIO71_PHY_RX_D3	GEM3
MIO_75	D29	MIO75_PHY_RX_CTRL	GEM3
MIO_76	E28	MIO76_PHY_MDC	GEM3
MIO_77	E25	MIO77_PHY_MDIO	GEM3

QSPI Flash

SMF_HSIO_HT3 provides 2 Micron MT25QU256ABA Flash chips (U13, U14) with total 512Mb (32 M x 8bit x 2) storage for MPSoC system to reserve boot image files. For higher performance, these two Quad-SPI chips are connected in parallel to provide 8-bit data bus for booting and configuration while this interface is default for supporting QSPI32 boot mode. This Quad-SPI interface is connected to Zynq UltraScale+ MPSoC bank 500 I/O pins with 1.8V voltage level.

Trace Name	FPGA Pin	QPSI Flash		
		Pin Name	Pin Number	Chip
MIO0_QSPI0_SCLK	H17	C	6	U13
MIO1_QSPI0_IO0	J17	DQ0	5	U13
MIO2_QSPI0_IO1	A20	DQ1	2	U13
MIO3_QSPI0_IO2	B19	DQ2/W#	3	U13
MIO4_QSPI0_IO3	D19	DQ3/HOLD#	7	U13
MIO5_QSPI0_CS#	C19	S#	1	U13
MIO7_QSPI0_SCLK	H18	C	6	U14
MIO8_QSPI0_IO0	E20	DQ0	5	U14
MIO9_QSPI0_IO1	F20	DQ1	2	U14
MIO10_QSPI0_IO2	F18	DQ2/W#	3	U14
MIO11_QSPI0_IO3	G18	DQ3/HOLD#	7	U14
MIO12_QSPI0_CS#	E19	S#	1	U14

MicroSD Card Interface

SMF_HSIO_HT3 provides a secure digital input/output (SDIO) interface as non-volatile memory access. This interface is default for supporting SD1_LS boot mode. The SDIO signal is connected to Zynq UltraScale+ MPSoC Bank 501 I/O pins with 3.3V voltage level.

Trace Name	FPGA Pin	microSD Card Interface	
		Pin Name	Pin Number
MIO44_SDIO_WP	E24	-	NC
MIO45_SDIO_CD	F23	C/D	9
MIO46_SDIO_D0	K20	DATA0	7
MIO47_SDIO_D1	K21	DATA1	8
MIO48_SDIO_D2	J21	DATA2	1
MIO49_SDIO_D3	G21	DATA3	2
MIO50_SDIO_CMD	J20	CMD	3
MIO51_SDIO_CLK	H21	CLK	5

USB-to-UART

SMF_HSIO_HT3 provides a USB-to-UART Bridge function, the USB signals are input from the micro USB port (USB2) and then through the CP2104 chip to transform USB protocol into UART. The UART signals are connected to MPSoC PS side.

Trace Name	CP2104-F03-GM (U12)		FPGA Pin
	Pin Number	Pin Name	
UART_D+	3	D+	
UART_D-	4	D-	
	20	RXD	B24(PS_MIO35)
	21	TXD	B23(PS_MIO34)

USB

SMF_HSIO_HT3 provides 1 USB 2.0/3.0 port. Through UTMI+ low pin interface (ULPI) USB2.0 PHY chip (USB3320C-EZK). USB2.0 signals are output directly through USB2.0 Type-A Connector while USB3.0 signals are through a PS GTR High-speed Transceiver and then output through USB3.0 Type-A Connector. USB interface is connected to Zynq UltraScale+ MPSoC bank 500, 502 I/O pins with 1.8V voltage level.

Trace Name	USB3320C-EZK(U10)		FPGA Pin
	Pin Number	Pin Name	
MIO56_USB_D0	3	D0	A25(PS_MIO56)
MIO57_USB_D1	4	D1	A26(PS_MIO57)
MIO54_USB_D2	5	D2	A23(PS_MIO54)
MIO59_USB_D3	6	D3	A27(PS_MIO59)
MIO60_USB_D4	7	D4	C26(PS_MIO60)
MIO61_USB_D5	9	D5	B29(PS_MIO61)
MIO62_USB_D6	10	D6	B28(PS_MIO62)
MIO63_USB_D7	13	D7	A29(PS_MIO63)
MIO52_USB_CLK	1	CLKOUT	A24(PS_MIO52)
MIO55_USB_NXT	2	NXT	B26(PS_MIO55)
MIO58_USB_STP	29	STP	A28(PS_MIO58)
MIO53_USB_DIR	31	DIR	B25(PS_MIO53)
USB_RESET#	27	RESET#	C18(PS_MIO17)

Audio

SMF_HSIO_HT3 provides an Audio function: The U17 TLV320AIC3111 features a high-performance audio codec with 16-bit stereo playback and monaural record functionality. The device integrates several analog features, such as a microphone interface, headphone drivers, and speaker drivers. TLV320A chip supports 8 KHz~192KHz ADC/DAC sampling rate and volume control. The Audio interface uses I2C for data transmission and is connected to Zynq UltraScale+ MPSoC bank 64 I/O pins with 3.3V voltage level.

Trace Name	Connected to	Bank Voltage
TLV320A_RSTn	B20(PS_MIO26)	
TLV320A_SDA	U32 SD0	
TLV320A_SCL	U32 SC0	
TLV320A_MCLK	A17	1.8V
TLV320A_DOUT	B16	1.8V
TLV320A_WCLK	D15	1.8V
TLV320A_DIN	C17	1.8V
TLV320A_BCLK	E15	1.8V

Programmable Frequency Clocks

SMF_HSIO_HT3 uses a Silicon Labs SI5340A-D-GM chip to generate arbitrary clock frequencies which are controlled by 4-Channel I2C Switch (TCA9546APWR)

Trace Name	SI5340A-D-GM(U24)		FPGA
	Pin Name	Pin Number	
SI5340A_SDA	SDA	13	J19(PS_MIO15)
SI5340A_SCL	SCL	14	E18(PS_MIO14)
MIO39_SI5340A_RST_N	RSTN	17	E22(PS_MIO39)
MIO40_SI5340A_OE_N	OEb	12	C24(PS_MIO40)
GTR_REF_DP_CLK_P	OUT0	20	L25 (PS_MGTREFCLK1P_505)
GTR_REF_DP_CLK_N	OUT0b	19	L26 (PS_MGTREFCLK1N_505)
GTR_REF_USB30_CLK_P	OUT1	25	M23 (PS_MGTREFCLK0P_505)
GTR_REF_USB30_CLK_N	OUT1b	24	M24 (PS_MGTREFCLK0N_505)
FPGA_CLK125_P	OUT2	31	E17
FPGA_CLK125_N	OUT2b	30	D17
HT3_C0P/ HT3_C1P	OUT3	36	
HT3_C0N/ HT3_C1N	OUT3b	35	
Trace Name	**SI570 (U27)**		**Connected to**
	Pin Name	**Pin Number**	
Default clock frequency : 156.25MHz			
SI570A_SDA	SDA	7	U32 SD2
SI570A_SCL	SCL	8	U32 SC2
FIREFLY_REFCLK_P	CLK+	4	MGTREFCLK0P_223/224/225/226
FIREFLY_REFCLK_N	CLK-	5	MGTREFCLK0N_223/224/225/226

I2C

I2C is through TCA9546APWR 4-Channel I2C Switch to control Programmable Frequency Clocks, SI570 I2C and INA226 I2C, separately.

Trace Name	TCA9546APWR(U32)		Connected To
	Pin Name	Pin Number	
MIO15_I2C0_SDA	SDA	15	J19(PS_MIO15)
MIO14_I2C0_SCL	SCL	14	E18(PS_MIO14)
MIO16_I2C0_RST_N	RSTN	3	K17(PS_MIO16)
TLV320A_SDA	SD0	4	U17 TLV320A
TLV320A_SCL	SC0	5	U17 TLV320A
SI5340A_SDA	SD1	6	U24 SI5340
SI5340A_SCL	SC1	7	U24 SI5340
SI570_SDA	SD2	9	U27 SI570
SI570_SCL	SC2	10	U27 SI570
INA226_SDA	SD3	11	U33 INA226
INA226_SCL	SC3	12	U33 INA226

Mini Display Port

SMF_HSIO_HT3 provides a Mini Display Port output controller which can support up to 2 channels. According to DisplayPort, the auxiliary channel signal DisplayPort AUX Channel (DPAUX) will use LVDS signal and are connected to Bank 501 with 3.3V voltage level.

Trace Name	FPGA Pin
DP_TX_P0	M27(PS_MGTRTXP0_505)
DP_TX_N0	M28(PS_MGTRTXN0_505)
DP_TX_P1	K27(PS_MGTRTXP1_505)
DP_TX_N1	K28(PS_MGTRTXN1_505)
MIO27_DP_AUX_OUT	B21(PS_MIO27)
MIO28_DP_HPD	A21(PS_MIO28)
MIO29_DP_OE	D21(PS_MIO29)
MIO30_DP_AUX_IN	C21(PS_MIO30)

Ethernet Port

SMF_HSIO_HT3 uses DP83867IRRGZR to realize the 10/100/1000 Ethernet port. There are two status indication light for RJ-45: flow indication and connection-status indication. This PS PHY is connected to Bank 502 with 1.8V voltage level.

Schematic Net Name	High Immunity 10/100/1000 Ethernet Physical Layer Transceiver(U9)		FPGA
	Pin Number	Pin Name	
MIO64_PHY_TX_CLK	29	TX_CLK	B30
MIO65_PHY_TX_D0	28	TXD0	D25
MIO66_PHY_TX_D1	27	TXD1	C27
MIO67_PHY_TX_D2	26	TXD2	C28
MIO68_PHY_TX_D3	25	TXD3	C29
MIO69_PHY_TX_CTRL	37	TX_CTRL	D27
MIO70_PHY_RX_CLK	32	RX_CLK	D26
MIO71_PHY_RX_D0	33	RXD0	D30
MIO72_PHY_RX_D1	34	RXD1	E27
MIO73_PHY_RX_D2	35	RXD2	E30
MIO74_PHY_RX_D3	36	RXD3	E29
MIO75_PHY_RX_CTRL	38	RX_CTRL	D29
MIO76_PHY_MDC	16	MDC	E28
MIO77_PHY_MDIO	17	MDIO	E25
MIO18_ETH_RESET#	43	RESET#	K18

FIREFLY Connector

FIREFLY Connector J8

Connector J8		U1	Connector J8		U1
Pin	Trace Name	Connected to	Pin	Trace Name	Connected to
A1	GND		B1	GND	
A2	FIREFLYA_TXD_N0	MGTHTXN3_226	B2	FIREFLYA_TXD_N1	MGTHTXN2_226
A3	FIREFLYA_TXD_P0	MGTHTXP3_226	B3	FIREFLYA_TXD_P1	MGTHTXP2_226
A4	GND		B4	GND	
A5	FIREFLYA_TXD_N2	MGTHTXN1_226	B5	FIREFLYA_TXD_N3	MGTHTXN0_226
A6	FIREFLYA_TXD_P2	MGTHTXP1_226	B6	FIREFLYA_TXD_P3	MGTHTXP0_226
A7	GND		B7	GND	
A8			B8		
A9			B9		
A10	GND		B10	GND	
A11			B11		
A12			B12		
A13	GND		B13	GND	
A14	FIREFLYA_RXD_P3	MGTHRXP0_226	B14	FIREFLYA_RXD_P2	MGTHRXP1_226
A15	FIREFLYA_RXD_N3	MGTHRXN0_226	B15	FIREFLYA_RXD_N2	MGTHRXN1_226
A16	GND		B16	GND	
A17	FIREFLYA_RXD_P1	MGTHRXP2_226	B17	FIREFLYA_RXD_P0	MGTHRXP3_226
A18	FIREFLYA_RXD_N1	MGTHRXN2_226	B18	FIREFLYA_RXD_N0	MGTHRXN3_226
A19	GND		B19	GND	

FIREFLY Connector J9

Connector J9		U1	Connector J9		U1
Pin	Trace Name	Connected to	Pin	Trace Name	Connected to
A1	GND		B1	GND	
A2	FIREFLYB_TXD_N0	MGTHTXN3_225	B2	FIREFLYB_TXD_N1	MGTHTXN2_225
A3	FIREFLYB_TXD_P0	MGTHTXP3_225	B3	FIREFLYB_TXD_P1	MGTHTXP2_225
A4	GND		B4	GND	
A5	FIREFLYB_TXD_N2	MGTHTXN1_225	B5	FIREFLYB_TXD_N3	MGTHTXN0_225
A6	FIREFLYB_TXD_P2	MGTHTXP1_225	B6	FIREFLYB_TXD_P3	MGTHTXP0_225
A7	GND		B7	GND	
A8			B8		
A9			B9		
A10	GND		B10	GND	
A11			B11		
A12			B12		
A13	GND		B13	GND	
A14	FIREFLYB_RXD_P3	MGTHRXP0_225	B14	FIREFLYB_RXD_P2	MGTHRXP1_225
A15	FIREFLYB_RXD_N3	MGTHRXN0_225	B15	FIREFLYB_RXD_N2	MGTHRXN1_225
A16	GND		B16	GND	
A17	FIREFLYB_RXD_P1	MGTHRXP2_225	B17	FIREFLYB_RXD_P0	MGTHRXP3_225
A18	FIREFLYB_RXD_N1	MGTHRXN2_225	B18	FIREFLYB_RXD_N0	MGTHRXN3_225
A19	GND		B19	GND	

FIREFLY Connector J10

Connector J10		U1	Connector J10		U1
Pin	Trace Name	Connected to	Pin	Trace Name	Connected to
A1	GND		B1	GND	
A2	FIREFLYC_TXD_N0	MGTHTXN3_224	B2	FIREFLYC_TXD_N1	MGTHTXN2_224
A3	FIREFLYC_TXD_P0	MGTHTXP3_224	B3	FIREFLYC_TXD_P1	MGTHTXP2_224
A4	GND		B4	GND	
A5	FIREFLYC_TXD_N2	MGTHTXN1_224	B5	FIREFLYC_TXD_N3	MGTHTXN0_224
A6	FIREFLYC_TXD_P2	MGTHTXP1_224	B6	FIREFLYC_TXD_P3	MGTHTXP0_224
A7	GND		B7	GND	
A8			B8		
A9			B9		
A10	GND		B10	GND	
A11			B11		
A12			B12		
A13	GND		B13	GND	
A14	FIREFLYC_RXD_P3	MGTHRXP0_224	B14	FIREFLYC_RXD_P2	MGTHRXP1_224
A15	FIREFLYC_RXD_N3	MGTHRXN0_224	B15	FIREFLYC_RXD_N2	MGTHRXN1_224
A16	GND		B16	GND	
A17	FIREFLYC_RXD_P1	MGTHRXP2_224	B17	FIREFLYC_RXD_P0	MGTHRXP3_224
A18	FIREFLYC_RXD_N1	MGTHRXN2_224	B18	FIREFLYC_RXD_N0	MGTHRXN3_224
A19	GND		B19	GND	

FIREFLY Connector J11

Connector J11		U1	Connector J11		U1
Pin	Trace Name	Connected to	Pin	Trace Name	Connected to
A1	GND		B1	GND	
A2	FIREFLYD_TXD_N0	MGTHTXN3_223	B2	FIREFLYD_TXD_N1	MGTHTXN2_223
A3	FIREFLYD_TXD_P0	MGTHTXP3_223	B3	FIREFLYD_TXD_P1	MGTHTXP2_223
A4	GND		B4	GND	
A5	FIREFLYD_TXD_N2	MGTHTXN1_223	B5	FIREFLYD_TXD_N3	MGTHTXN0_223
A6	FIREFLYD_TXD_P2	MGTHTXP1_223	B6	FIREFLYD_TXD_P3	MGTHTXP0_223
A7	GND		B7	GND	
A8			B8		
A9			B9		
A10	GND		B10	GND	
A11			B11		
A12			B12		
A13	GND		B13	GND	
A14	FIREFLYD_RXD_P3	MGTHRXP0_223	B14	FIREFLYD_RXD_P2	MGTHRXP1_223
A15	FIREFLYD_RXD_N3	MGTHRXN0_223	B15	FIREFLYD_RXD_N2	MGTHRXN1_223
A16	GND		B16	GND	
A17	FIREFLYD_RXD_P1	MGTHRXP2_223	B17	FIREFLYD_RXD_P0	MGTHRXP3_223
A18	FIREFLYD_RXD_N1	MGTHRXN2_223	B18	FIREFLYD_RXD_N0	MGTHRXN3_223
A19	GND		B19	GND	

HT3 Connector

JX1

JX1 (A0-B13)							JX1 (C0-D13)					
Pin	Trace Name			Connected to	Bank		Pin	Trace Name			Connected to	Bank
A0	HT3A_A0	VCCO	U1	AJ10	65		C0	HT3A_C0	VCCO	U1	AK7	65
A1	HT3A_A1			AK10			C1	HT3A_C1			AK6	
A2	HT3A_A2			AG8			C2	HT3A_C2			AH6	
A3	HT3A_A3			AH8			C3	HT3A_C3			AJ6	
A4	HT3A_A4			AG11			C4	HT3A_C4			AJ4	
A5	HT3A_A5			AH11			C5	HT3A_C5			AK4	
A6	HT3A_A6			AJ11			C6	HT3A_C6			AJ5	
A7	HT3A_A7			AK11			C7	HT3A_C7			AK5	
A8	HT3A_A8			AH12			C8	HT3A_C8			AK3	
A9	HT3A_A9			AJ12			C9	HT3A_C9			AK2	
A10	HT3A_A10			AF12			C10	HT3A_C10			AF6	
A11	HT3A_A11			AF11			C11	HT3A_C11			AF5	
A12	HT3A_A12			AG9			C12					
A13							C13					
B0	HT3A_B0			AE9	65		D0	HT3A_D0			AJ2	65
B1	HT3A_B1			AE8			D1	HT3A_D1			AJ1	
B2	HT3A_B2			AH7			D2	HT3A_D2			AG6	
B3	HT3A_B3			AJ7			D3	HT3A_D3			AG5	
B4	HT3A_B4			AH9			D4	HT3A_D4			AG4	
B5	HT3A_B5			AJ9			D5	HT3A_D5			AG3	
B6	HT3A_B6			AF8			D6	HT3A_D6			AH3	
B7	HT3A_B7			AF7			D7	HT3A_D7			AH2	
B8	HT3A_B8			AF10			D8	HT3A_D8			AF3	
B9	HT3A_B9			AG10			D9	HT3A_D9			AF2	
B10	HT3A_B10			AK9			D10	HT3A_D10			AG1	
B11	HT3A_B11			AK8			D11	HT3A_D11			AH1	
B12							D12	HT3A_D12			AF1	
B13							D13					

JX2

JX2 (A0-B13)							JX2 (C0-D13)					
Pin	Trace Name			Connected to	Bank		Pin	Trace Name			Connected to	Bank
A0	HT3B_A0	1.8V	U1	D14	46		C0	HT3B_C0	1.8V	U1	G13	46
A1	HT3B_A1			C13			C1	HT3B_C1			F13	
A2	HT3B_A2	1.2V		AD1	66		C2	HT3B_C2	1.2V		AJ16	64
A3	HT3B_A3			AE1			C3	HT3B_C3			AK16	
A4	HT3B_A4			AC3			C4	HT3B_C4			AH17	
A5	HT3B_A5			AC2			C5	HT3B_C5			AJ17	
A6	HT3B_A6			AA3			C6	HT3B_C6			AK17	
A7	HT3B_A7			AB3			C7	HT3B_C7			AK18	
A8	HT3B_A8			AB1			C8	HT3B_C8			AG18	
A9	HT3B_A9			AC1			C9	HT3B_C9			AH18	
A10	HT3B_A10			AA2			C10	HT3B_C10			AE18	
A11	HT3B_A11			AA1			C11	HT3B_C11			AF18	
A12	HT3B_A12			Y1			C12					
A13							C13					
B0	HT3B_B0	1.8V		E14	46		D0	HT3B_D0	1.8V		F12	46
B1	HT3B_B1			E13			D1	HT3B_D1			E12	
B2	HT3B_B2	1.2V		AA15	64		D2	HT3B_D2	1.2V		AB10	66
B3	HT3B_B3			AB15			D3	HT3B_D3			AB9	
B4	HT3B_B4			AA14			D4	HT3B_D4			AD11	
B5	HT3B_B5			AB14			D5	HT3B_D5			AD10	
B6	HT3B_B6			AC14			D6	HT3B_D6			AB11	
B7	HT3B_B7			AD14			D7	HT3B_D7			AC11	
B8	HT3B_B8			AE14			D8	HT3B_D8			AA12	
B9	HT3B_B9			AE13			D9	HT3B_D9			AA11	
B10	HT3B_B10			AA13			D10	HT3B_D10			AC12	
B11	HT3B_B11			AB13			D11	HT3B_D11			AD12	
B12							D12	HT3B_D12			W9	
B13							D13					

HSIO Connector

J4

Connector J4		U1			Connector J4		U1		
Pin	Trace Name	Connected to	Bank Voltage	Bank	Pin	Trace Name	Connected to	Bank Voltage	Bank
1	HSIOA_DATA_N0	AE4	1.2V	66	2	HSIOA_CLK_N0	AE7	1.2V	66
3	HSIOA_DATA_P0	AD4			4	HSIOA_CLK_P0	AD7		
5	GND				6	GND			
7	GND				8	GND			
9	HSIOA_DATA_N1	AC4	1.2V	66	10	HSIOA_DATA_N3	AA5	1.2V	66
11	HSIOA_DATA_P1	AB4			12	HSIOA_DATA_P3	AA6		
13	GND				14	GND			
15	GND				16	GND			
17	HSIOA_DATA_N2	AE5	1.2V	66	18	HSIOA_DATA_N4	AB5	1.2V	66
19	HSIOA_DATA_P2	AD5			20	HSIOA_DATA_P4	AB6		
21	GND				22	GND			
23	GND				24	GND			
25	HSIOA_GPIO0	Y10	1.2V	66	26	HSIOA_GPIO3	K11	1.8V	46
27	GND				28	GND			
29	GND				30	GND			
31	HSIOA_GPIO1	AA10	1.2V	66	32	HSIOA_GPIO4	AD2	1.2V	66
33	GND				34	GND			
35	GND				36	GND			
37	HSIOA_GPIO2	AE2	1.2V	66	38	HSIOA_GPIO5	K12	1.8V	46
39	GND				40	GND			

J5

Connector J5		U1			Connector J5		U1		
Pin	Trace Name	Connected to	Bank Voltage	Bank	Pin	Trace Name	Connected to	Bank Voltage	Bank
1	HSIOB_DATA_N0	AD6	1.2V	66	2	HSIOB_CLK_N0	AB8	1.2V	66
3	HSIOB_DATA_P0	AC6			4	HSIOB_CLK_P0	AA8		
5	GND				6	GND			
7	GND				8	GND			
9	HSIOB_DATA_N1	AD9	1.2V	66	10	HSIOB_DATA_N3	Y8	1.2V	66
11	HSIOB_DATA_P1	AC9			12	HSIOB_DATA_P3	W8		
13	GND				14	GND			
15	GND				16	GND			
17	HSIOB_DATA_N2	AC7	1.2V	66	18	HSIOB_DATA_N4	AA7	1.2V	66
19	HSIOB_DATA_P2	AC8			20	HSIOB_DATA_P4	Y7		
21	GND				22	GND			
23	GND				24	GND			
25	HSIOB_GPIO0	AE15	1.2V	64	26	HSIOB_GPIO3	C12	1.8V	46
27	GND				28	GND			
29	GND				30	GND			
31	HSIOB_GPIO1	C14	1.8V	46	32	HSIOB_GPIO4	B14	1.8V	46
33	GND				34	GND			
35	GND				36	GND			
37	HSIOB_GPIO2	AD15	1.2V	64	38	HSIOB_GPIO5	D12	1.8V	46
39	GND				40	GND			

J6

Connector J6		U1			Connector J6		U1		
Pin	Trace Name	Connected to	Bank Voltage	Bank	Pin	Trace Name	Connected to	Bank Voltage	Bank
1	HSIOC_DATA_N0	AE17	1.2V	64	2	HSIOC_CLK_N0	AF17	1.2V	64
3	HSIOC_DATA_P0	AD17			4	HSIOC_CLK_P0	AF16		
5	GND				6	GND			
7	GND				8	GND			
9	HSIOC_DATA_N1	AD16	1.2V	64	10	HSIOC_DATA_N3	AB16	1.2V	64
11	HSIOC_DATA_P1	AC16			12	HSIOC_DATA_P3	AA16		
13	GND				14	GND			
15	GND				16	GND			
17	HSIOC_DATA_N2	AE19	1.2V	64	18	HSIOC_DATA_N4	AC18	1.2V	64
19	HSIOC_DATA_P2	AD19			20	HSIOC_DATA_P4	AC17		
21	GND				22	GND			
23	GND				24	GND			
25	HSIOC_GPIO0	AH16	1.2V	64	26	HSIOC_GPIO3	A14	1.8V	46
27	GND				28	GND			
29	GND				30	GND			
31	HSIOC_GPIO1	B12	1.8V	46	32	HSIOC_GPIO4	A13	1.8V	46
33	GND				34	GND			
35	GND				36	GND			
37	HSIOC_GPIO2	AG16	1.2V	64	38	HSIOC_GPIO5	A12	1.8V	46
39	GND				40	GND			

J7

Connector J7		U1			Connector J7		U1		
Pin	Trace Name	Connected to	Bank Voltage	Bank	Pin	Trace Name	Connected to	Bank Voltage	Bank
1	HSIOD_DATA_N0	AK12	1.2V	64	2	HSIOD_CLK_N0	AG15	1.2V	64
3	HSIOD_DATA_P0	AK13			4	HSIOD_CLK_P0	AF15		
5	GND				6	GND			
7	GND				8	GND			
9	HSIOD_DATA_N1	AK15	1.2V	64	10	HSIOD_DATA_N3	AH14	1.2V	64
11	HSIOD_DATA_P1	AJ15			12	HSIOD_DATA_P3	AG14		
13	GND				14	GND			
15	GND				16	GND			
17	HSIOD_DATA_N2	AK14	1.2V	64	18	HSIOD_DATA_N4	AH13	1.2V	64
19	HSIOD_DATA_P2	AJ14			20	HSIOD_DATA_P4	AG13		
21	GND				22	GND			
23	GND				24	GND			
25	HSIOD_GPIO0	J12	1.8V	46	26	HSIOD_GPIO3	H14	1.8V	46
27	GND				28	GND			
29	GND				30	GND			
31	HSIOD_GPIO1	K13	1.8V	46	32	HSIOD_GPIO4	H13	1.8V	46
33	GND				34	GND			
35	GND				36	GND			
37	HSIOD_GPIO2	H12	1.8V	46	38	HSIOD_GPIO5	G14	1.8V	46
39	GND				40	GND			