SOC_DBG_HT3
EH2012003030
Reference Manual

March 2021 ver0.4

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E-ELEMENTS TECHNOLOGY CO., LTD.

5F, No.61, Lane76, RuiguangRd.,

Neihu Dist., Taipei,

Taiwan, R.O.C.

www.e-elements.com

Revision History

Date	Rev	Comment
Jun 2020	V0.1	Initial version.
Nov 2020	V0.2	Change the ping of nSRST and nTRST.
Jan 2021	V0.3	Add the Level shift in block diagram.
Mar 2021	V0.4	Correct the Mitctor38 and MIPI60 connected to JX1 Pin

Contents

IMPORTANT!

ESD

The SOC_DBG_HT3 Transceiver Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

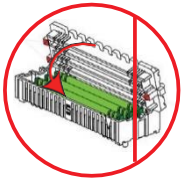
- Transport the card in an ESD bag
- Wear an anti-static wrist strap
- Make sure the work area is equipped with an ESD mat

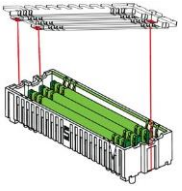
Warning

Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS® system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

HapsTrak® 3 Connector Considerations

The HT3 connectors must be attached carefully! If connected improperly socket pins can be deformed or holding rail ends can become damaged.





Overview

This document is the SOC_DBG_HT3 Reference Manual and describes the functions of the SOC_DBG_HT3 daughter board.

The SOC_DBG_HT3 daughter board includes one Type-C USB connector providing four RS-232 connection through a standard USB cable, connectivity for 20-pin ARM Cortex Debug interface, 38-pin MICTOR and 28-pin PMOD interface with GPIO interface.

Figure 1: Top View of SOC_DBG_HT3 daughter board

SOC_DBG_HT3 daughter board consists of:

- 3 8-pin + 1 4-pin 3.3V-level GPIO Headers
- 1 20-pin ARM Cortex Debug + ETM Connector
- 1 Type-C USB Ports
- 1 38-pin MICTOR Connector
- 1 12-pin Pad for Other GPIO
- 1 60-pin MIPI60 Connector

Layout

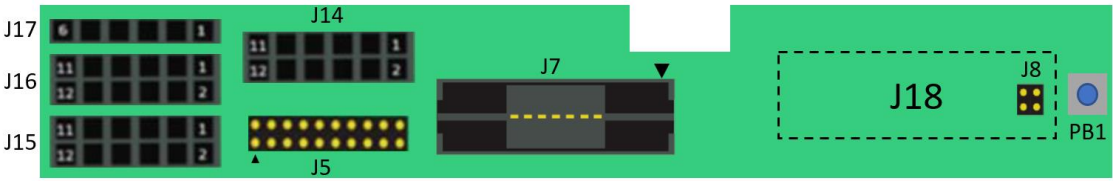


Figure 2: Top and Bottom(dotted line) of SOC_DBG_HT3 stacked board layout

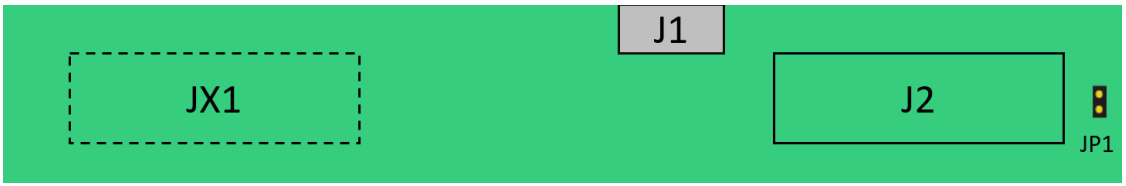


Figure 3: Top and Bottom(dotted line) of SOC_DBG_HT3 base board layout

Block Diagram

Figure 4 show the connectivity between the SOC_DBG_HT3 daughter board's headers and connectors to the HT3 connector. The HT3 I/O pin mapping is described in the JX1 pin table on page 14.

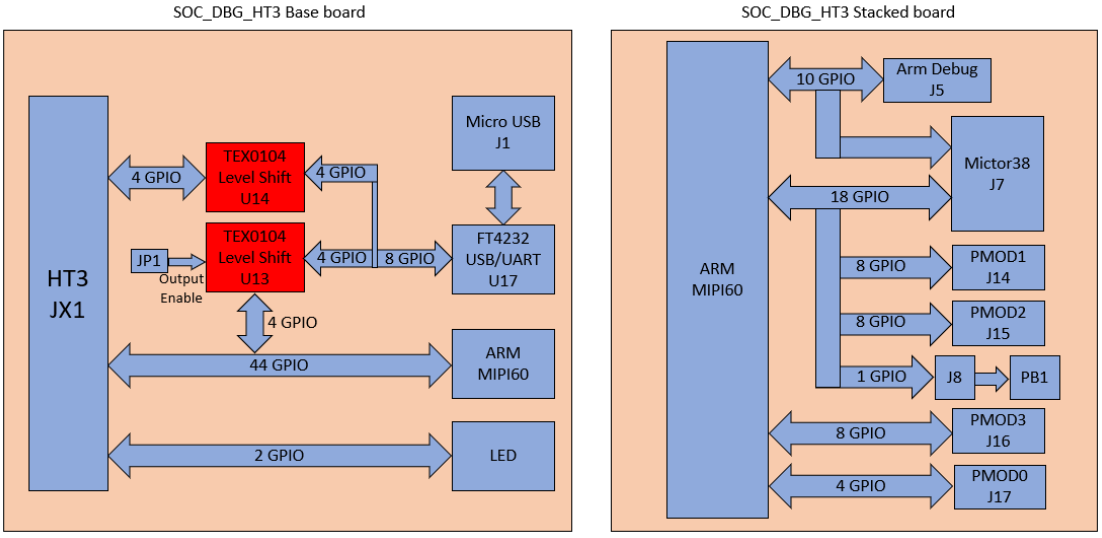


Figure 4: SOC_DBG_HT3 Block Diagram

Daughter Board Placement

HAPS-80 systems include 24 HT3 Connector for each FPGA. The HapsTrak 3 (HT3) is a 160-pin connector containing 52 signal pins, most of which can be used for single ended or differential signaling. All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

The SOC_DBG_HT3 card connected to HAPS-80 through HT3 connector, Figure 5 is the example of card installed.

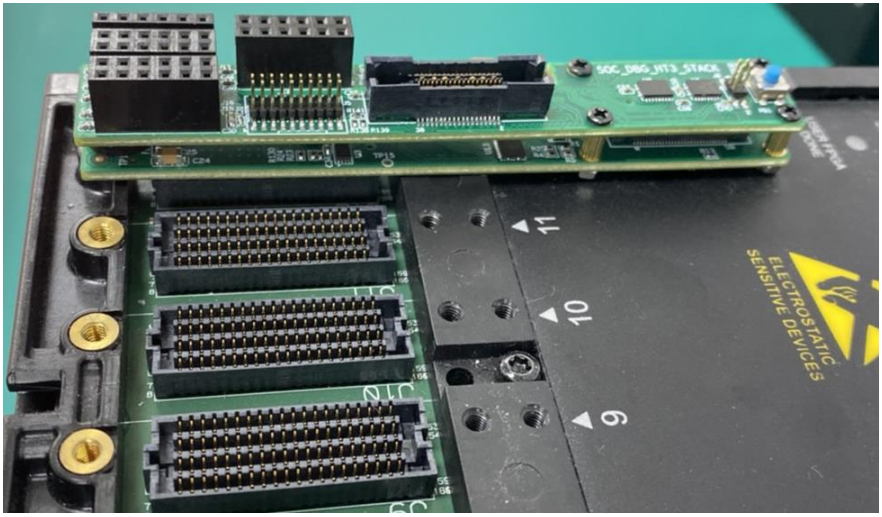


Figure 5: SOC_DBG_HT3 mounted on HAPS-80 system

HAPS GPIO Headers

Standard 3.3V GPIO Headers

Connectors J14, J15, J16 and J17 are standard 3.3V level HAPS GPIO Headers, which provide access to 28 FPGA I/O signals (8 I/O signals per connector). The I/O pins mapping are described on page14.

The GPIO headers are available for any design specific application including:

- Included LED/Button board
- I2C/SPI host adapter to access debug logic inside the FPGA (adapter cable may be required)
- PMOD modules (adapter cable required for module connectors, for this board application)

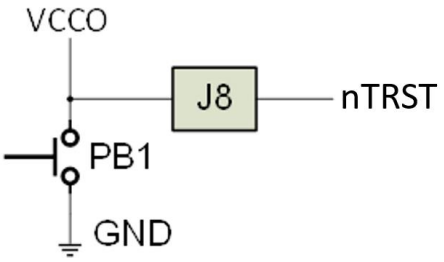
Jumpers

Jumpers provide different configuration options dependent on your requirements.

Jumper	Description
JP1	Short: U13 UART(TX2/RX2 and TX3/RX3) output disable. Open: U13 UART(TX2/RX2 and TX3/RX3) output enable.
J8	Short 1-2: connect to PB1(low active).

Button

Button PB1 can control Mictor pin nTRST, if push PB1 then nTRST be Low, else nTRST be High.



MICTOR

SOC_DBG_HT3 provides connectivity between MICTOR connector J7 to user FPGA I/O pins through the HT3 connector. MICTOR are used in logic analyzers, and some of MICTOR signals can be used for JTAG ,e.g. in FPGA debugging variants of the connector.

Part: CONN HEADER Mictor 38 SMT
Number: AMP 5767056-1
Web address: te.com

ARM Debug Interface

SOC_DBG_HT3 provides connectivity between connector J5 to user FPGA I/O pins through the HT3 connector. J5 is a 20-pin header with ground and signals arranged for ARM debug interface. Connect the proper signals in the user FPGA design from the FPGA internal ARM core debug ports to the HT3 pins according to the pin mapping depicted in the JX1 pin table on page 14. The ten I/Os allocated to this interface are routed to the ARM connector from GPIO Header JX1 and are also available for alternate uses.

Type-C USB Port

The Type-C USB connector provides four RS-232 connection through a standard USB cable to your host computer. Designs that utilize an UART module may connect to the USB/UART pins to be accessed and controlled through a terminal application.

FTDI FT4232HQ is used to bridge UART and USB. Download and install the Virtual COM port (VCP) driver from ftdichip.com. The driver allows the USB device to appear as a COM port available to the host computer. Application software can access the USB device in the same way as it would access a standard COM port.

Part: USB to serial UART Interface
Number: FT4232HQ
Web address: ftdichip.com

Note: VCCO must be configured to 1.8V

Pin Tables

HT3 Connector

JX1							
(A0-B13)				(C0-D13)			
Pin	Trace Name	Connector		Pin	Trace Name	Connector	
A0	TRACE_D15	J2	VCCO	C0	TRACE_CLK0	J2	VCCO
A1	TRACE_D14			C1	UART_TXD1	J1	VCCO
A2	TRACE_D13			C2	UART_RXD1		
A3	TRACE_D12			C3	TDI_NC	J2	VCCO
A4	TRACE_D11			C4	UART_TX3	J1	VCCO
					TRACE_D31	J2	VCCO
A5	TRACE_D10			C5	UART_RX3	J1	VCCO
					TRACE_D30	J2	VCCO
A6	TRACE_D9			C6	UART_TXD0	J1	VCCO
A7	TRACE_D8			C7	UART_RXD0		
A8	TRACE_D7			C8	TRACE_D27	J2	VCCO
A9	TRACE_D6			C9	TRACE_D26		
A10	TRACE_D5			C10	TRACE_D25		
A11	TRACE_D4			C11	TRACE_D24		
A12	LED0	D3	VCCO	C12			
A13				C13			
B0	RTCK	J2	VCCO	D0	TCK_SWDCLK	J2	VCCO
B1	TRST_PD_exTRIG			D1	TMS_SWDIO		
B2	DBGRQ			D2	TRACE_CTL		
B3	DBGACK			D3	TDO_SWO		
B4	TRACE_D23			D4	TRACE_D0		
B5	TRACE_D22			D5	nSRST / ARM_RESET_N		
B6	TRACE_D21			D6	UART_TX2	J1	VCCO
					TRACE_D29	J2	VCCO
B7	TRACE_D20			D7	UART_RX2	J1	VCCO
					TRACE_D28	J2	VCCO
B8	TRACE_D19			D8	TRACE_D3		
B9	TRACE_D18			D9	TRACE_D2		
B10	TRACE_D17			D10	TRACE_D1		
B11	TRACE_D16			D11	nTRST		
B12				D12	LED1	D4	VCCO
B13				D13			

	J1 UART
	J2 MIPI60
	D3/D4 LED

ARM MIPI60

JX1	J2(Base board)/J18(Stacked board)				JX1
-	VCCO	1	2	TMS_SWDIO	D1
D0	TCK_SWDCLK	3	4	TDO_SWO	D3
C3	TDI_NC	5	6	nSRST	D5
B0	RTCK	7	8	TRST_PD_exTRIG	B1
D11	nTRST	9	10	DBGRQ	B2
B3	DBGACK	11	12	VCCO	-
C0	TRACE_CLK0	13	14	NC	-
-	GND	15	16	GND	-
D2	TRACE_CTL	17	18	TRACE_D19	B8
D4	TRACE_D0	19	20	TRACE_D20	B7
D10	TRACE_D1	21	22	TRACE_D21	B6
D9	TRACE_D2	23	24	TRACE_D22	B5
D8	TRACE_D3	25	26	TRACE_D23	B4
A11	TRACE_D4	27	28	TRACE_D24	C11
A10	TRACE_D5	29	30	TRACE_D25	C10
A9	TRACE_D6	31	32	TRACE_D26	C9
A8	TRACE_D7	33	34	TRACE_D27	C8
A7	TRACE_D8	35	36	TRACE_D28	D7
A6	TRACE_D9	37	38	TRACE_D29	D6
A5	TRACE_D10	39	40	TRACE_D30	C5
A4	TRACE_D11	41	42	TRACE_D31	C4
A3	TRACE_D12	43	44	NC	-
A2	TRACE_D13	45	46	NC	-
A1	TRACE_D14	47	48	NC	-
A0	TRACE_D15	49	50	NC	-
B11	TRACE_D16	51	52	NC	-
B10	TRACE_D17	53	54	NC	-
B9	TRACE_D18	55	56	NC	-
-	GND	57	58	GND	-
-	NC	59	60	NC	-

ARM Cortex Debug+ETM Connector

J5(Stacked board)				JX1
VCCO	1	2	TMS_SDWIO	D1
GND	3	4	TCK _SWDCLK	D0
	5	6	TDO_ SWD	D3
	7	8	TDI _NC	C3
	9	10	ARM_RESET_N	D5
	11	12	TRACE_CLK	C0
	13	14	TRACE_D0	D4
	15	16	TRACE_D1	D10
	17	18	TRACE_D2	D9
	19	20	TRACE_D3	D8

MICTOR Connector

JX1	J7(Stacked board)				JX1
-	NC	1	2	NC	-
-	NC	3	4	NC	-
-	GND	5	6	TRACE_CLK	C0
B2	DBGRQ	7	8	DBGACK	B3
D5	ARM_RESET_N	9	10	TRST_PD_exTRIG	B1
D3	TDO_ SWO	11	12	VCCO	-
B0	RTCK	13	14	VCCO	-
D0	TCK_ SWDCLK	15	16	TRACE_D7	A8
D1	TMS_ SDWIO	17	18	TRACE_D6	A9
C3	TDI_NC	19	20	TRACE_D5	A10
D11	nTRST	21	22	TRACE_D4	A11
A0	TRACE_D15	23	24	TRACE_D3	D8
A1	TRACE_D14	25	26	TRACE_D2	D9
A2	TRACE_D13	27	28	TRACE_D1	D10
A3	TRACE_D12	29	30	GND	-
A4	TRACE_D11	31	32	GND	-
A5	TRACE_D10	33	34	VCCO	-
A6	TRACE_D9	35	36	Trace_CTL	D2
A7	TRACE_D8	37	38	TRACE_D0	D4

Jumpers

J8(Stacked board)			
PB1	1	2	nTRST
NC	3	4	NC

PMOD

JX1	J14(Stacked board)				JX1
A0	PMOD_IO1[0]	1	2	PMOD_IO1[1]	A1
A2	PMOD_IO1[2]	3	4	PMOD_IO1[3]	A3
A4	PMOD_IO1[4]	5	6	PMOD_IO1[5]	A5
A6	PMOD_IO1[6]	7	8	PMOD_IO1[7]	A7
-	GND	9	10	GND	-
-	3.3V	11	12	3.3V	-

JX1	J15(Stacked board)				JX1
A8	PMOD_IO2[0]	1	2	PMOD_IO2[1]	A9
A10	PMOD_IO2[2]	3	4	PMOD_IO2[3]	A11
B0	PMOD_IO2[4]	5	6	PMOD_IO2[5]	B1
B2	PMOD_IO2[6]	7	8	PMOD_IO2[7]	B3
-	GND	9	10	GND	-
-	3.3V	11	12	3.3V	-

JX1	J16(Stacked board)				JX1
B4	PMOD_IO3[0]	1	2	PMOD_IO3[1]	B5
B6	PMOD_IO3[2]	3	4	PMOD_IO3[3]	B7
B8	PMOD_IO3[4]	5	6	PMOD_IO3[5]	B9
B10	PMOD_IO3[6]	7	8	PMOD_IO3[7]	B11
-	GND	9	10	GND	-
-	3.3V	11	12	3.3V	-

JX1	J17(Stacked board)	
C8	PMOD_IO0[0]	1
C9	PMOD_IO0[1]	2
C10	PMOD_IO0[2]	3
C11	PMOD_IO0[3]	4
-	GND	5
-	3.3V	6