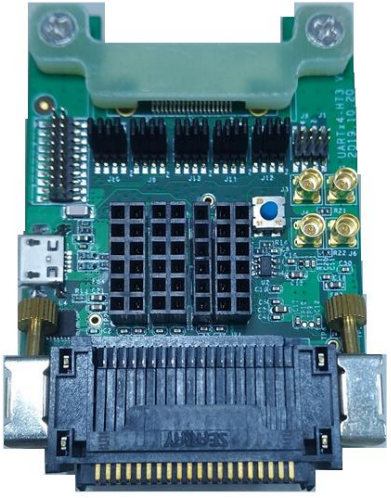
SOC_IOV_HT3
EH1803003016
Reference Manual

April 2020 ver2.2



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Revision History

Date	Rev	Comment
Feb 2018	v0	Initial version
Jul 2019	v1.1	Correct the connect name J11、J12 to J14、J15
Jul 2019	v1.2	Correct the UART pin name
Nov 2019	v1.3	Correct the Mictor38 pin in HT3
Nov 2019	v2.0	Modified the layout
Apr 2020	v2.1	Correct the HAPS GPIO Header connector describe
May 2020	v2.2	Correct the PMOD0 pin in HT3

Contents

IMPORTANT!

ESD

The SOC_IOV_HT3 Transceiver Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

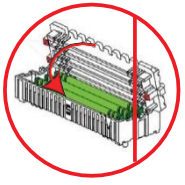
- Transport the card in an ESD bag
- Wear an anti-static wrist strap
- Make sure the work area is equipped with an ESD mat

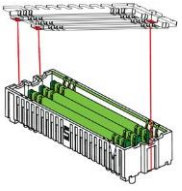
Warning

Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS® system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

HapsTrak® 3 Connector Considerations

The HT3 connectors must be attached carefully! If connected improperly socket pins can be deformed or holding rail ends can become damaged.





Overview

This document is the SOC_IOV_HT3 Reference Manual and describes the functions of the SOC_IOV_HT3 daughter board.

The SOC_IOV_HT3 daughter board includes one micro-USB connector providing four RS-232 connection through a standard USB cable, connectivity for 20-pin ARM Cortex Debug interface, 38-pin MICTOR and 28-pin PMOD interface with GPIO interface.

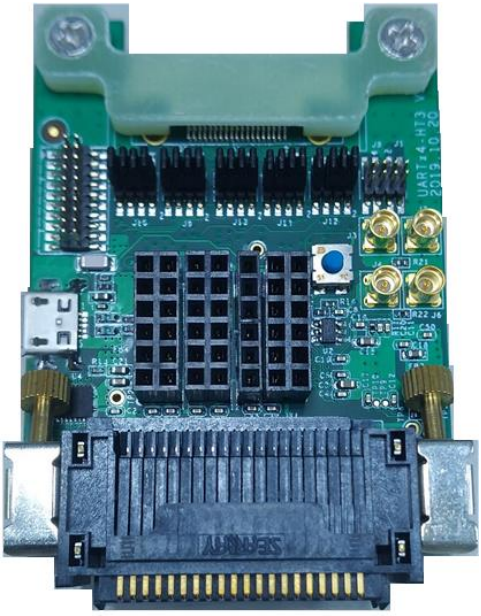


Figure 1: Top View of SOC_IOV_HT3 daughter board

SOC_IOV_HT3 daughter board consists of:

- 3 8-pin + 1 4-pin 3.3V-level GPIO Headers
- 5 8-pin VCCO-level to 3.3V GPIO Jumpers
- 1 20-pin ARM Cortex Debug + ETM Connector
- 1 Micro-USB Ports
- 2 pairs of Differential MMCX Clock Connectors (for Global Clocks)
- 1 38-pin MICTOR Connector
- 1 12-pin Pad for Other GPIO

Layout

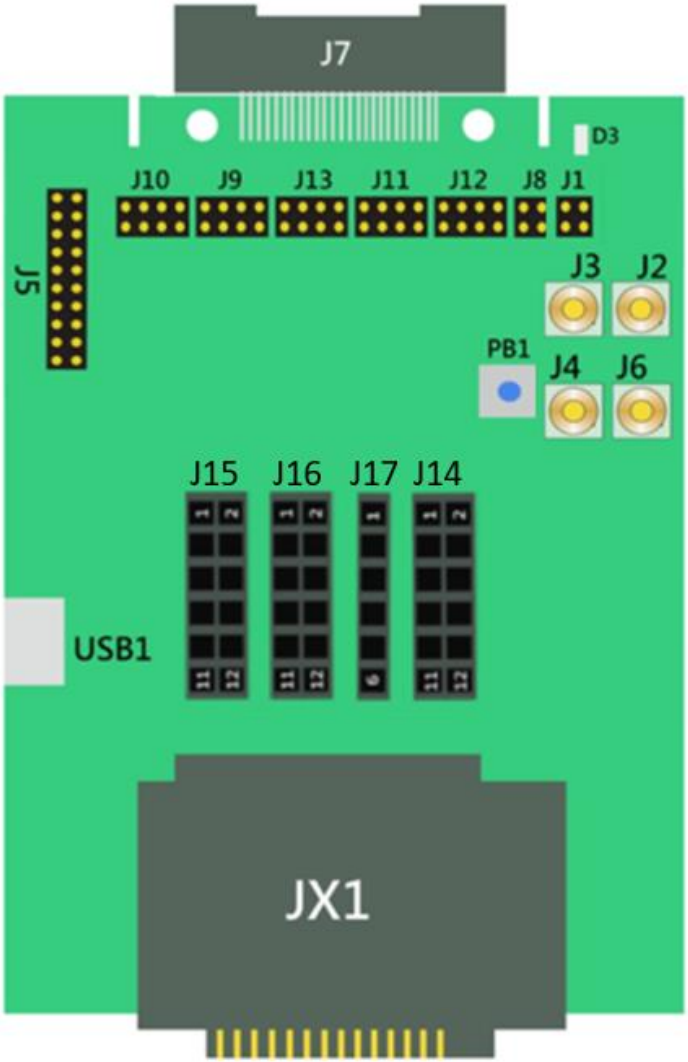


Figure 2: Top View of SOC_IOV_HT3 Layout

Block Diagram

Figure 3 show the connectivity between the SOC_IOV_HT3 daughter board's headers and connectors to the HT3 connector. The HT3 I/O pin mapping is described in the JX1 pin table on page 15.

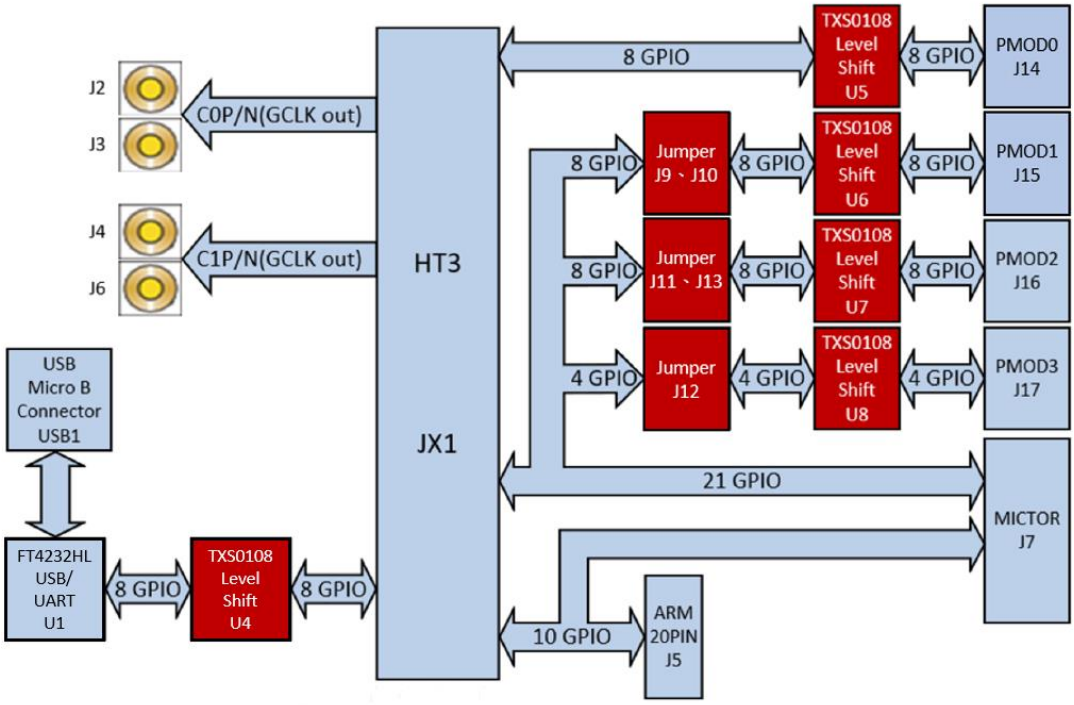


Figure 3: SOC_IOV_HT3 Block Diagram

Daughter Board Placement

HAPS-80 systems include 24 HT3 Connector for each FPGA. The HapsTrak 3 (HT3) is a 160-pin connector containing 52 signal pins, most of which can be used for single ended or differential signaling. All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

The SOC_IOV_HT3 card connected to HAPS-80 through HT3 connector, Figure 4 is the example of card installed.

Figure 4: SOC_IOV_HT3 mounted on HAPS-80 system

HAPS GPIO Headers

Standard 3.3V GPIO Headers

Connectors J14, J15, J16 and J17 are standard 3.3V level HAPS GPIO Headers, which provide access to 28 FPGA I/O signals (8 I/O signals per connector). The I/O pins mapping are described on page 17.

The GPIO headers are available for any design specific application including:

- Included LED/Button board
- I2C/SPI host adapter to access debug logic inside the FPGA (adapter cable may be required)
- PMOD modules (adapter cable required for module connectors, for this board application)

High-Speed VCCO GPIO Headers

Special high-speed VCCO level GPIO headers (J9, J10, J11, J12 and J13) allow access to FPGA I/O signals at a VCCO level. The I/O pins mapping are described on page 16.

Tables 1 list various ways of connecting the control signals using jumper headers available on the SOC_IOV_HT3 card

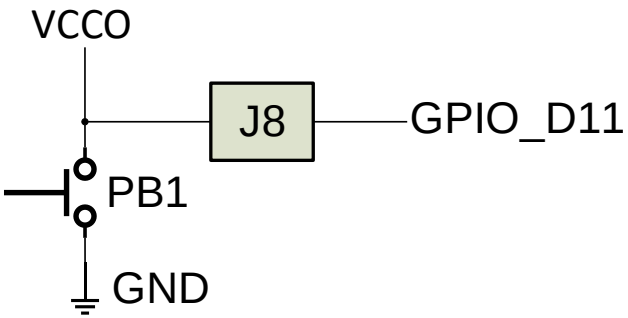
Control Pin	Jumper	Source Configuration	Control Pin	Jumper	Source Configuration
GPIO_A0	J9	Pin 1-2: J15 Output pin 1	GPIO_B0	J13	Pin 1-2: J16 Output pin 5
GPIO_A1	J9	Pin 3-4: J15 Output pin 2	GPIO_B1	J13	Pin 3-4: J16 Output pin 6
GPIO_A2	J9	Pin 5-6: J15 Output pin 3	GPIO_B2	J13	Pin 5-6: J16 Output pin 7
GPIO_A3	J9	Pin 7-8: J15 Output pin 4	GPIO_B3	J13	Pin 7-8: J16 Output pin 8
GPIO_A4	J10	Pin 1-2: J15 Output pin 5	GPIO_B4	J12	Pin 1-2: J17 Output pin 1
GPIO_A5	J10	Pin 3-4: J15 Output pin 6	GPIO_B5	J12	Pin 3-4: J17 Output pin 2
GPIO_A6	J10	Pin 5-6: J15 Output pin 7	GPIO_B6	J12	Pin 5-6: J17 Output pin 3
GPIO_A7	J10	Pin 7-8: J15 Output pin 8	GPIO_B7	J12	Pin 7-8: J17 Output pin 4
GPIO_A8	J11	Pin 1-2: J16 Output pin 1	GPIO_C5	J1	Pin 1-2: control LED D3
GPIO_A9	J11	Pin 3-4: J16 Output pin 2	GPIO_C5	J1	Pin 1-3: enable USB1 sleep pin
GPIO_A10	J11	Pin 5-6: J16 Output pin 3	3.3V	J1	Pin 2-4: show LED D3 for 3.3V
GPIO_A11	J11	Pin 7-8: J16 Output pin 4	PB1	J8	Pin 1-2: control FPGA GPIO_D11

Table 1: SOC_IOV_HT3 Control Signals

Part: CONN HEADER 8POS DUAL .05 SMD
Number: FTSH-104-01-F-DV
Web address: samtec.com

Button

Button PB1 can control FPGA GPIO_D11, if push PB1 then GPIO_D11 be Low, else GPIO_D11 be High.



MICTOR

SOC_IOV_HT3 provides connectivity between MICTOR connector J7 to user FPGA I/O pins through the HT3 connector. MICTOR are used in logic analyzers, and some of MICTOR signals can be used for JTAG ,e.g. in FPGA debugging variants of the connector.

Part: CONN HEADER Mictor 38 SMT
Number: AMP 2-5767004-2
Web address: te.com

ARM Debug Interface

SOC_IOV_HT3 provides connectivity between connector J5 to user FPGA I/O pins through the HT3 connector. J5 is a 20-pin header with ground and signals arranged for ARM debug interface. Connect the proper signals in the user FPGA design from the FPGA internal ARM core debug ports to the HT3 pins according to the pin mapping depicted in the JX1 pin table on page 18. The ten I/Os allocated to this interface are routed to the ARM connector from GPIO Header JX1 and are also available for alternate uses.

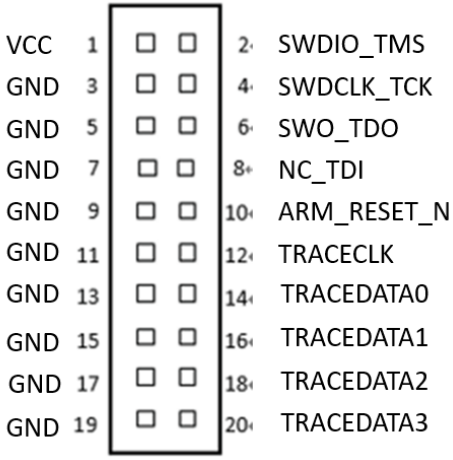


Figure 5: ARM 20-pin Cortex Debug + ETM Connector

Micro-USB Port

The micro-USB connector provides four RS-232 connection through a standard USB cable to your host computer. Designs that utilize an UART module may connect to the USB/UART pins to be accessed and controlled through a terminal application.

FTDI FX4232HL is used to bridge UART and USB. Download and install the Virtual COM port (VCP) driver from ftdichip.com. The driver allows the USB device to appear as a COM port available to the host computer. Application software can access the USB device in the same way as it would access a standard COM port.

Part: USB to serial UART Interface
Number: FT4232HL
Web address: ftdichip.com

Note: VCCO must be configured to 1.8V

Clocks

MMCX connectors for clock connections between the user FPGA and other components in a hardware setup.

Output Clocks

Output clocks are internal signals (FPGA generated clocks or HAPS global clocks) that travel from the HAPS system through the SOC_IOV_HT3 daughter board.

Access to the HAPS system's differential global clock (GCLK) signals are available through the Output clock SMB connector pairs on the SOC_IOV_HT3 daughter board. Table 1 is a list of clock connections for each MMCX connector.

MMCX Connector		Direction	Source
J2/J3	Differential	Output	C0P/C0N
J4/J6	Differential	Output	C1P/C1N

Table 2: MMCX Clock Connections

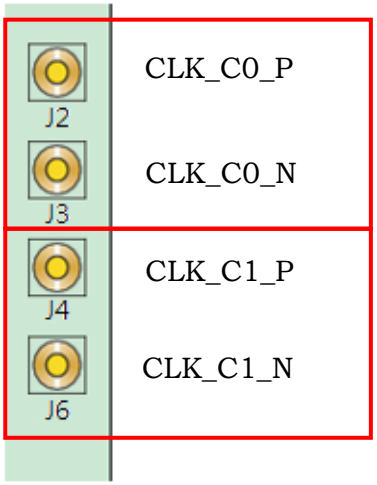


Figure 6: DIFF Clocks

Pin Tables

HT3 Connector

JX1								
(A0-B13)					(C0-C1P)			
Pin	Trace Name	Connector			Pin	Trace Name	Connector	
A0	TRACEDATA_15	J7	VCCO		C0	UART_TXD2	USB1	VCCC
	PMOD1_PIN1	J15	3.3V		C1	UART_TXD0		
A1	TRACEDATA_14	J7	VCCO		C2	UART_RXD0		
	PMOD1_PIN2	J15	3.3V		C3	UART_TXD3		
A2	TRACEDATA_13	J7	VCCO		C4	UART_RXD3		
	PMOD1_PIN3	J15	3.3V		C5	UART_SUSPEND_N		
A3	TRACEDATA_12	J7	VCCO			LED	D3	3.3V
	PMOD1_PIN4	J15	3.3V		C6	UART_TXD1	USB1	VCCC
A4	TRACEDATA_11	J7	VCCO		C7	UART_RXD1		
	PMOD1_PIN5	J15	3.3V		C8	PMOD0_PIN1	J14	3.3V
A5	TRACEDATA_10	J7	VCCO		C9	PMOD0_PIN2	J14	
	PMOD1_PIN6	J15	3.3V		C10	PMOD0_PIN3	J14	
A6	TRACEDATA_9	J7	VCCO		C11	PMOD0_PIN4	J14	
	PMOD1_PIN7	J15	3.3V		D0	UARD_RXD2	USB1	VCCC
A7	TRACEDATA_8	J7	VCCO		D1	SDWIO_TMS	J5	VCCC
	PMOD1_PIN8	J15	3.3V				J7	
A8	TRACEDATA_7	J7	VCCO		D2	SWDCLK_TCK	J5	
	PMOD2_PIN1	J16	3.3V				J7	
A9	TRACEDATA_6	J7	VCCO		D3	SWO_TDO	J5	
	PMOD2_PIN2	J16	3.3V				J7	
A10	TRACEDATA_5	J7	VCCO		D4	NC_TDI	J5	
	PMOD2_PIN3	J16	3.3V				J7	
A11	TRACEDATA_4	J7	VCCO		D5	ARM_RESET_N	J5	
	PMOD2_PIN4	J16	3.3V				J7	
A12	TP_DIP	TP13	3.3V		D6	TRACECLK	J5	
B0	LOGIC00	J7	VCCO				J7	
	PMOD2_PIN5	J16	3.3V		D7	TRACEDATA_0	J5	
B1	LOGIC01	J7	VCCO				J7	
	PMOD2_PIN6	J16	3.3V		D8	TRACEDATA_1	J5	
B2	LOGIC10	J7	VCCO				J7	
	PMOD2_PIN7	J16	3.3V		D9	TRACEDATA_2	J5	
B3	TraceCTL	J7	VCCO				J7	
	PMOD2_PIN8	J16	3.3V		D10	TRACEDATA_3	J5	
B4	DBGRQ	J7	VCCO				J7	
	PMOD3_PIN1	J17	3.3V		D11	nTRST	J7	
B5	RTCK	J7	VCCO		D12	UART_PWREN_N	USB1	3.3V
	PMOD3_PIN2	J17	3.3V		C0N	CLK_C0_N	J3	VCCO
B6	DBGACK	J7	VCCO		C0P	CLK_C0_P	J2	VCCO
	PMOD3_PIN3	J17	3.3V		C1N	CLK_C1_N	J6	VCCO
B7	EXTTRIG	J7	VCCO		C1P	CLK_C1_P	J4	VCCO
	PMOD3_PIN4	J17	3.3V					
B8	PMOD0_PIN5	J14	3.3V					
B9	PMOD0_PIN6	J14	3.3V					
B10	PMOD0_PIN7	J14	3.3V					
B11	PMOD0_PIN8	J14	3.3V					

	J5 ARM Dedug		TP13 TP_DIP
	D3 LED		J12/J16/J17/J11
	USB1 USB		J2/J3/J4/J6
	J7 Mictor		Differential

Jumpers

J8			
VCCO	1	2	nTRST
NC	3	4	NC

J1			
GPIO_C5	1	2	LED3
SUSPEND_N	3	4	3.3V

	J9 VCCO		U6
GPIO_A0	1	2	GPIO_A0
GPIO_A1	3	4	GPIO_A1
GPIO_A2	5	6	GPIO_A2
GPIO_A3	7	8	GPIO_A3

	J10 VCCO		U6
GPIO_A4	1	2	GPIO_A4
GPIO_A5	3	4	GPIO_A5
GPIO_A6	5	6	GPIO_A6
GPIO_A7	7	8	GPIO_A7

	J11 VCCO		U7
GPIO_A8	1	2	GPIO_A8
GPIO_A9	3	4	GPIO_A9
GPIO_A10	5	6	GPIO_A10
GPIO_A11	7	8	GPIO_A11

	J13 VCCO		U7
GPIO_B0	1	2	GPIO_B0
GPIO_B1	3	4	GPIO_B1
GPIO_B2	5	6	GPIO_B2
GPIO_B3	7	8	GPIO_B3

	J12 VCCO		U8
GPIO_B4	1	2	GPIO_B4
GPIO_B5	3	4	GPIO_B5
GPIO_B6	5	6	GPIO_B6
GPIO_B7	7	8	GPIO_B7

MICTOR Connector

J7			
NC	1	2	NC
NC	3	4	NC
GND	5	6	TRACECLK
DBGRQ	7	8	DBGACK
ARM_RST_N	9	10	extTRIG
SWO_TDO	11	12	VCCO
RTCK	13	14	VCCO
SWDCLK_TCLK	15	16	TRACEDATA_7
SDWIO_TMS	17	18	TRACEDATA_6
NC_TDI	19	20	TRACEDATA_5
nTRST	21	22	TRACEDATA_4
TRACEDATA_15	23	24	TRACEDATA_3
TRACEDATA_14	25	26	TRACEDATA_2
TRACEDATA_13	27	28	TRACEDATA_1
TRACEDATA_12	29	30	Logic00
TRACEDATA_11	31	32	Logic01
TRACEDATA_10	33	34	Logic10
TRACEDATA_9	35	36	TraceCTL
TRACEDATA_8	37	38	TRACEDATA_0

PMOD

PMOD_IO0					
Board file trace name	U5	J14 3.3V		U5	Board file trace name
PMOD_IO0[0]	GPIO_C8	1	2	GPIO_C9	PMOD_IO0[1]
PMOD_IO0[2]	GPIO_C10	3	4	GPIO_C11	PMOD_IO0[3]
PMOD_IO0[4]	GPIO_B8	5	6	GPIO_B9	PMOD_IO0[5]
PMOD_IO0[6]	GPIO_B10	7	8	GPIO_B11	PMOD_IO0[7]
	GND	9	10	GND	
	3.3V	11	12	3.3V	

PMOD_IO1					
Board file trace name	U6	J15 3.3V		U6	Board file trace name
PMOD_IO1[0]	GPIO_A0	1	2	GPIO_A1	PMOD_IO1[1]
PMOD_IO1[2]	GPIO_A2	3	4	GPIO_A3	PMOD_IO1[3]
PMOD_IO1[4]	GPIO_A4	5	6	GPIO_A5	PMOD_IO1[5]
PMOD_IO1[6]	GPIO_A6	7	8	GPIO_A7	PMOD_IO1[7]
	GND	9	10	GND	
	3.3V	11	12	3.3V	

PMOD_IO2					
Board file trace name	U7	J16 3.3V		U7	Board file trace name
PMOD_IO2[0]	GPIO_A8	1	2	GPIO_A9	PMOD_IO2[1]
PMOD_IO2[2]	GPIO_A10	3	4	GPIO_A11	PMOD_IO2[3]
PMOD_IO2[4]	GPIO_B0	5	6	GPIO_B1	PMOD_IO2[5]
PMOD_IO2[6]	GPIO_B2	7	8	GPIO_B3	PMOD_IO2[7]
	GND	9	10	GND	
	3.3V	11	12	3.3V	

PMOD_IO3		
Board file trace name	U8	J17 3.3V
PMOD_IO3[0]	GPIO_B4	1
PMOD_IO3[1]	GPIO_B5	2
PMOD_IO3[2]	GPIO_B6	3
PMOD_IO3[3]	GPIO_B7	4
	GND	5
	3.3V	6

ARM Cortex Debug+ETM Connector

J5			
VCCO	1	2	SDWIO_TMS
GND	3	4	SWDCLK_TCLK
	5	6	SWD_TDO
	7	8	NC_TDI
	9	10	ARM_RST_N
	11	12	TRACECLK
	13	14	TRACEDATA_0
	15	16	TRACEDATA_1
	17	18	TRACEDATA_2
	19	20	TRACEDATA_3

FT4232HL USB/UART

	U4		U1 Pin Name
GPIO_C1	1	11	GND
VCCO	2	12	UART_RXD3
GPIO_C2	3	13	UART_TXD3
GPIO_C6	4	14	UART_RXD2
GPIO_C7	5	15	UART_TXD2
GPIO_C0	6	16	UART_RXD1
GPIO_D0	7	17	UART_TXD1
GPIO_C3	8	18	UART_RXD0
GPIO_C4	9	19	3.3V
VCCO	10	20	UART_TXD0

Micro USB Connector

U1	USB1		
VCCO	1	5	GND
BM	2	6	
BP	3	7	
NC	4	8	