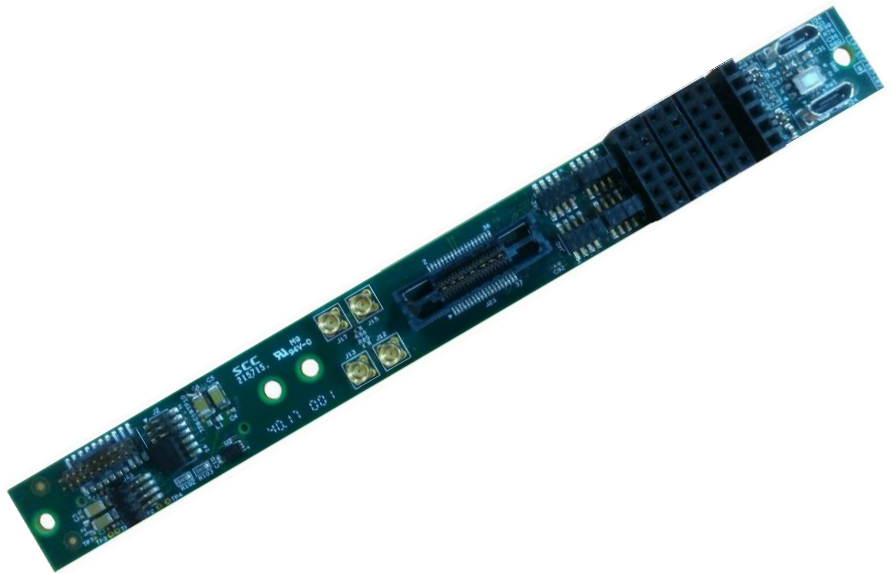


SOC_IO_HT3 EH1705003015 Reference Manual

November 2017 ver0.1



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Revision History

Date	Rev	Comment
Nov 2017	v0	Initial version

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SOC_IO_HT3

IMPORTANT!

ESD



The SOC_IO_HT3 Transceiver Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

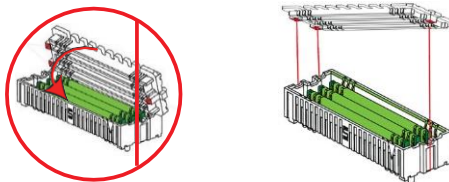
- Transport the card in an ESD bag
- Wear an anti-static wrist strap
- Make sure the work area is equipped with an ESD mat

Warning

Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS[®] system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

HapsTrak[®] 3 Connector Considerations

The HT3 connectors must be attached carefully! If connected improperly socket pins can be deformed or holding rail ends can become damaged.



Overview

This document is the SOC_IO_HT3 Reference Manual and describes the functions of the SOC_IO_HT3 daughter board.

The SOC_IO_HT3 daughter board includes two micro-USB connectors providing an RS-232 connection through a standard USB cable, connectivity for 20-pin ARM Cortex Debug interface, 38-pin MICTOR and 28-pin PMOD interface with GPIO interface.

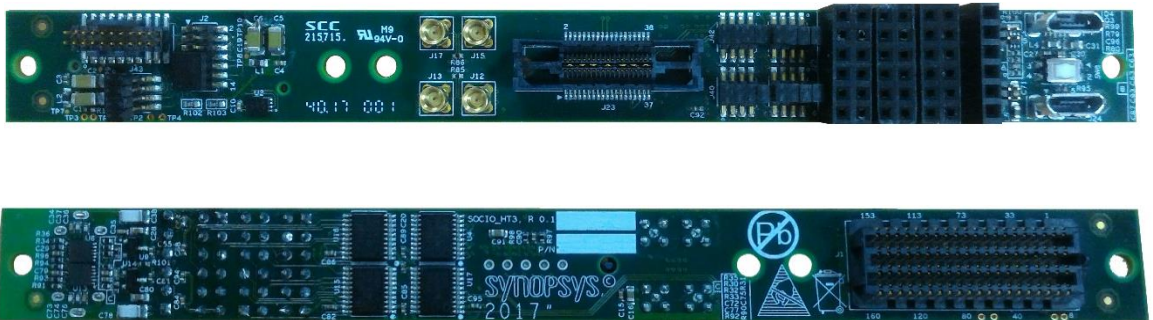


Figure 1: Top and Bottom View of SOC_IO_HT3 daughter board

SOC_IO_HT3 daughter board consists of:

- 3 8-pin + 1 4-pin 3.3V-level GPIO Headers
- 5 8-pin VCCO-level to 3.3V GPIO Jumpers
- 1 20-pin ARM Cortex Debug + ETM Connector
- 2 Micro-USB Ports
- 2 pairs of Differential MMCX Clock Connectors (for Global Clocks)
- 1 38-pin MICTOR Connector
- 1 12-pin Pad for Other GPIO

Layout

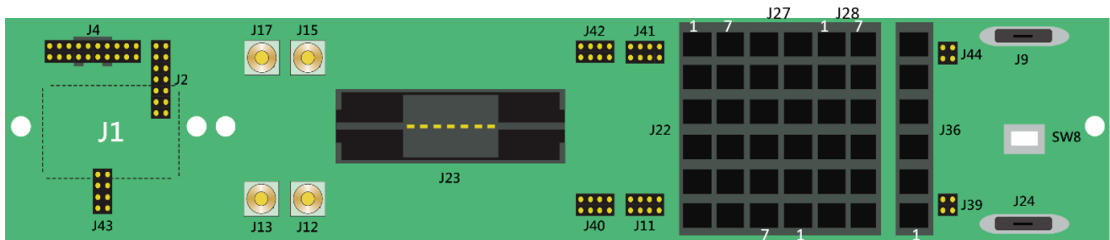


Figure 2: Top and Bottom (dotted line) SOC_IO_HT3 Layout

Block Diagram

Figure 3 show the connectivity between the SOC_IO_HT3 daughter board's headers and connectors to the HT3 connector. The HT3 I/O pin mapping is described in the J1 pin table on page 15.

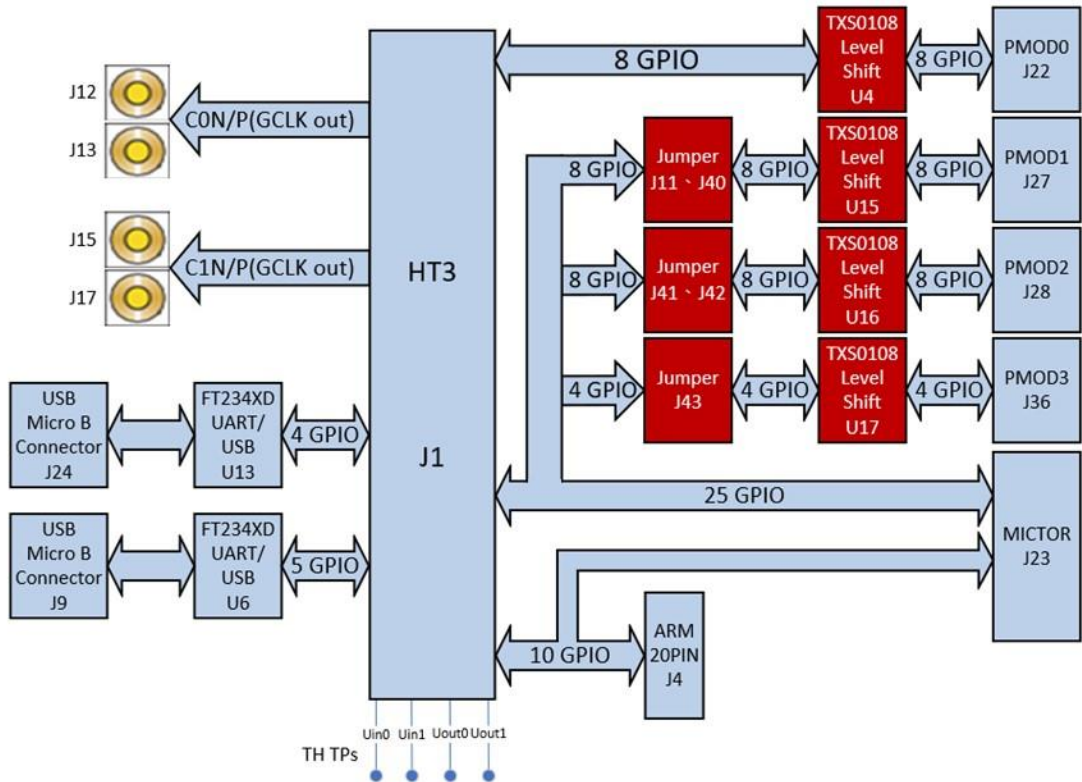


Figure 3: SOC_IO_HT3 Block Diagram

Daughter Board Placement

HAPS-80 systems include 24 HT3 Connector for each FPGA. The HapsTrak 3 (HT3) is a 160-pin connector containing 52 signal pins, most of which can be used for single ended or differential signaling. All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

The SOC_IO_HT3 card connected to HAPS-80 through HT3 connector, Figure 4 is the example of card installed



Figure 4: SOCIO_HT3 mounted on HAPS-80 system

HAPS GPIO Headers

Standard 3.3V GPIO Headers

Connectors J22, J27, J28 and J36 are standard 3.3V level HAPS GPIO Headers, which provide access to 28 FPGA I/O signals (8 I/O signals per connector). The I/O pins mapping are described on page 17.

The GPIO headers are available for any design specific application including:

- Included LED/Button board
- I2C/SPI host adapter to access debug logic inside the FPGA (adapter cable may be required)
- PMOD modules (adapter cable required for module connectors, for this board application)

High-Speed VCCO GPIO Headers

Special high-speed VCCO level GPIO headers (J11, J40, J41, J42 and J43) allow access to FPGA I/O signals at a VCCO level. The I/O pins mapping are described on page 16.

Tables 1 list various ways of connecting the control signals using jumper headers available on the SOC_IO_HT3 card

Control Pin	Jumper	Source Configuration	Control Pin	Jumper	Source Configuration
GPIO_A0	J11	Pin 1-2: J27 Output pin 1	GPIO_B0	J42	Pin 1-2: J28 Output pin 7
GPIO_A1	J11	Pin 3-4: J27 Output pin 2	GPIO_B1	J42	Pin 3-4: J28 Output pin 8
GPIO_A2	J11	Pin 5-6: J27 Output pin 3	GPIO_B2	J42	Pin 5-6: J28 Output pin 9
GPIO_A3	J11	Pin 7-8: J27 Output pin 4	GPIO_B3	J42	Pin 7-8: J28 Output pin 10
GPIO_A4	J40	Pin 1-2: J27 Output pin 7	GPIO_B4	J43	Pin 1-2: J36 Output pin 1
GPIO_A5	J40	Pin 3-4: J27 Output pin 8	GPIO_B5	J43	Pin 3-4: J36 Output pin 2
GPIO_A6	J40	Pin 5-6: J27 Output pin 9	GPIO_B6	J43	Pin 5-6: J36 Output pin 3
GPIO_A7	J40	Pin 7-8: J27 Output pin 10	GPIO_B7	J43	Pin 7-8: J36 Output pin 4
GPIO_A8	J41	Pin 1-2: J28 Output pin 1			
GPIO_A9	J41	Pin 3-4: J28 Output pin 2			
GPIO_A10	J41	Pin 5-6: J28 Output pin 3			
GPIO_A11	J41	Pin 7-8: J28 Output pin 4			

Table 1: SOCIO_HT3 Control Signals

Part: CONN HEADER 8POS DUAL .05 SMD

Number: FTSH-104-01-F-DV

Web address: samtec.com

MICTOR

SOC_IO_HT3 provides connectivity between MICTOR connector J23 to user FPGA I/O pins through the HT3 connector. MICTOR are used in logic analyzers, and some of MICTOR signals can be used for JTAG ,e.g. in FPGA debugging variants of the connector.

Part: CONN HEADER Mictor 38 SMT

Number: AMP 2-5767004-2

Web address: te.com

ARM Debug Interface

SOC_IO_HT3 provides connectivity between connector J4 to user FPGA I/O pins through the HT3 connector. J4 is a 20-pin header with ground and signals arranged for ARM debug interface. Connect the proper signals in the user FPGA design from the FPGA internal ARM core debug ports to the HT3 pins according to the pin mapping depicted in the J1 pin table on page 17. The ten I/Os allocated to this interface are routed to the ARM connector from GPIO Header J1 and are also available for alternate uses.

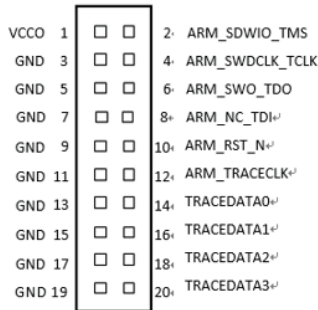


Figure 5: ARM 20-pin Cortex Debug + ETM Connector

Micro-USB Port

The micro-USB connector provides an RS-232 connection through a standard USB cable to your host computer. Designs that utilize an UART module may connect to the USB/UART pins to be accessed and controlled through a terminal application.

FTDI FX234XD is used to bridge UART and USB. Download and install the Virtual COM port (VCP) driver from ftdichip.com. The driver allows the USB device to appear as a COM port available to the host computer. Application software can access the USB device in the same way as it would access a standard COM port.

Part: USB to serial UART Interface

Number: FT234XD

Web address: ftdichip.com

Note: VCCO must be configured to 1.8V

Clocks

MMCX connectors for clock connections between the user FPGA and other components in a hardware setup.

Output Clocks

Output clocks are internal signals (FPGA generated clocks or HAPS global clocks) that travel from the HAPS system through the SOCIO_HT3 daughter board.

Access to the HAPS system's differential global clock (GCLK) signals are available through the Output clock SMB connector pairs on the SOCIO_HT3 daughter board. Table 1 is a list of clock connections for each MMCX connector.

MMCX Connector		Direction	Source
J12/J13	Differential	Output	C0P/C0N
J15/J17	Differential	Output	C1P/C1N

Table 2: MMCX Clock Connections

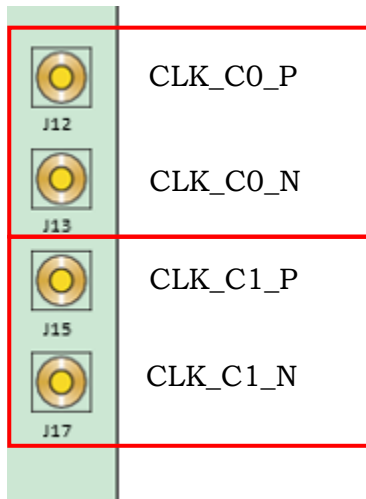


Figure 6: DIFF Clocks

Pin Tables

HT3 Connector

J1																					
(A0-B13)					(C0-C1P)																
Pin	Trace Name	Connector			Pin	Trace Name	Connector														
A0	TRACEDATA_15	J23	VCCO		C0	UART0_RTS_N	J24	USB													
	PMOD1_PIN1	J27	3.3V		C1	UART1_TXD	J9														
A1	TRACEDATA_14	J23	VCCO		C2	UART1_RXD							J9								
	PMOD1_PIN2	J27	3.3V		C3	UART1_RTS_N															
A2	TRACEDATA_13	J23	VCCO		C4	UART1_CTS_N							J9								
	PMOD1_PIN3	J27	3.3V		C5	UART1_SLEEP_N															
A3	TRACEDATA_12	J23	VCCO			LED4	D4	VCCO/3.3													
	PMOD_PIN4	J27	3.3V		C6	UART0_TXD	J24	USB													
A4	TRACEDATA_11	J23	VCCO		C7	UART0_RXD	J22	3.3V													
	PMOD1_PIN7	J27	3.3V		C8	PMOD0_PIN1	J22														
A5	TRACEDATA_10	J23	VCCO		C9	PMOD0_PIN2	J22						J2	VCCO							
	PMOD1_PIN8	J27	3.3V		C10	PMOD0_PIN3	J22														
A6	TRACEDATA_9	J23	VCCO		C11	PMOD0_PIN4	J22	J24	USB												
	PMOD1_PIN9	J27	3.3V		C12	RSIG3	J2														
A7	TRACEDATA_8	J23	VCCO		C13	RSIG7		J24													
	PMOD1_PIN10	J27	3.3V		D0	UART0_CTS_N	J4							VCCO							
A8	TRACEDATA_7	J23	VCCO		D1	SDWIO_TMS	J23														
	PMOD2_PIN1	J28	3.3V		D2	SWDCLK_TCK	J4														
A9	TRACEDATA_6	J23	VCCO				J23														
	PMOD2_PIN2	J28	3.3V		D3	SWO_TDO	J4														
A10	TRACEDATA_5	J23	VCCO				J23														
	PMOD2_PIN3	J28	3.3V	D4	NC_TDI	J4															
A11	TRACEDATA_4	J23	VCCO			J23															
	PMOD2_PIN4	J28	3.3V	D5	RST_N	J4															
A12	RSIG1	J2	VCCO			J23															
A13	RSIG5			D6	TRACECLK	J4															
B0	LOGIC00	J23	VCCO			J23															
	PMOD2_PIN7	J28	3.3V	D7	TRACEDATA_0	J4															
B1	LOGIC01	J23	VCCO			J23															
	PMOD2_PIN8	J28	3.3V	D8	TRACEDATA_1	J4															
B2	LOGIC10	J23	VCCO			J23															
	PMOD2_PIN9	J28	3.3V	D9	TRACEDATA_2	J4															
B3	TraceCTL	J23	VCCO			J23															
	PMOD2_PIN10	J28	3.3V	D10	TRACEDATA_3	J4															
B4	DBGREQ	J23	VCCO			J23															
	PMOD3_PIN1	J36	3.3V	D11	nTRST	J23															
B5	RTCK	J23	VCCO	D12	RSIG4	J2								VCCO							
	PMOD3_PIN2	J36	3.3V	D13	RSIG8																
B6	exTRIG	J23	VCCO	CON	CLK_CO_N	J13		1.8V						DIFF							
	PMOD3_PIN3	J36	3.3V	C0P	CLK_CO_P	J12															
B7	DBGACK	J23	VCCO	C1N	CLK_C1_N	J17															
	PMOD3_PIN4	J36	3.3V	C1P	CLK_C1_P	J15															
B8	PMOD0_PIN7	J22	3.3V																		
B9	PMOD0_PIN8	J22	3.3V																		
B10	PMOD0_PIN9	J22	3.3V																		
B11	PMOD0_PIN10	J22	3.3V																		
B12	RSIG2	J2	VCCO																		
B13	RSIG6																				

J4 ARM

D4 LED

J9/J24 USB

J23 Mictor

J27/J28/J36/J22

Other-GPIO

J12/J13/J15/J17

Differential Clocks

Other GPIO Connector

J2			
RSIG1	1	2	RSIG7
RSIG2	3	4	RSIG8
RSIG3	5	6	RSB1
RSIG4	7	8	RSB2
RSIG5	9	10	RSB3
RSIG6	11	12	RESET_N
GPIO_VRP	13	14	GPIO_VRN

Jumpers

J39			
VCCO	1	2	nTRST
NC	3	4	NC

J44			
GPIO_C5	1	2	LED4
UART1_SLEEP_N	3	4	3.3V

	J11 VCCO		U15
GPIO_A0	1	2	GPIO_A0
GPIO_A1	3	4	GPIO_A1
GPIO_A2	5	6	GPIO_A2
GPIO_A3	7	8	GPIO_A3

	J40 VCCO		U15
GPIO_A4	1	2	GPIO_A4
GPIO_A5	3	4	GPIO_A5
GPIO_A6	5	6	GPIO_A6
GPIO_A7	7	8	GPIO_A7

	J41 VCCO		U16
GPIO_A8	1	2	GPIO_A8
GPIO_A9	3	4	GPIO_A9
GPIO_A10	5	6	GPIO_A10
GPIO_A11	7	8	GPIO_A11

	J42 VCCO		U16
GPIO_B0	1	2	GPIO_B0
GPIO_B1	3	4	GPIO_B1
GPIO_B2	5	6	GPIO_B2
GPIO_B3	7	8	GPIO_B3

	J43 VCCO		U17
GPIO_B4	1	2	GPIO_B4
GPIO_B5	3	4	GPIO_B5
GPIO_B6	5	6	GPIO_B6
GPIO_B7	7	8	GPIO_B7

MICTOR Connector

J23			
NC	1	2	NC
NC	3	4	NC
GND	5	6	TRACECLK
DBGREQ	7	8	DBGACK
ARM_RST_N	9	10	extTRIG
SWO_TDO	11	12	VCCO
RTCK	13	14	VCCO
SWDCLK_TCLK	15	16	TRACEDATA_7
SDWIO_TMS	17	18	TRACEDATA_6
NC_TDI	19	20	TRACEDATA_5
nTRST	21	22	TRACEDATA_4
TRACEDATA_15	23	24	TRACEDATA_3
TRACEDATA_14	25	26	TRACEDATA_2
TRACEDATA_13	27	28	TRACEDATA_1
TRACEDATA_12	29	30	Logic00
TRACEDATA_11	31	32	Logic01
TRACEDATA_10	33	34	Logic10
TRACEDATA_9	35	36	TraceCTL
TRACEDATA_8	37	38	TRACEDATA_0
GND	39	40	GND
GND	41	42	GND
GND	43	44	NC

PMOD

U4	J22 3.3V		U4
GPIO_C8	1	7	GPIO_B8
GPIO_C9	2	8	GPIO_B9
GPIO_C10	3	9	GPIO_B10
GPIO_C11	4	10	GPIO_B11
GND	5	11	GND
3.3V	6	12	3.3V

U15	J27 3.3V		U15
GPIO_A0	1	7	GPIO_A4
GPIO_A1	2	8	GPIO_A5
GPIO_A2	3	9	GPIO_A6
GPIO_A3	4	10	GPIO_A7
GND	5	11	GND
3.3V	6	12	3.3V

U16	J28 3.3V		U16
GPIO_A8	1	7	GPIO_B0
GPIO_A9	2	8	GPIO_B1
GPIO_A10	3	9	GPIO_B2
GPIO_A11	4	10	GPIO_B3
GND	5	11	GND
3.3V	6	12	3.3V

U17	J36 3.3V		U17
GPIO_B4	1	7	NC
GPIO_B5	2	8	NC
GPIO_B6	3	9	NC
GPIO_B7	4	10	NC
GND	5	11	NC
3.3V	6	12	NC

ARM Cortex Debug+ETM Connector

J4			
VCCO	1	2	SDWIO_TMS
GND	3	4	SWDCLK_TCLK
	5	6	SWD_TDO
	7	8	NC_TDI
	9	10	ARM_RST_N
	11	12	TRACECLK
	13	14	TRACEDATA_0
	15	16	TRACEDATA_1
	17	18	TRACEDATA_2
	19	20	TRACEDATA_3

FT234XD UART/USB

	U13		
DATA_N	1	8	GPIO_C0
OUT_N	2	9	VCCO
GND	3	10	GPIO_C7
OUT_N	4	11	GPIO_D0
GND	5	12	DATA_P
NC	6	13	GND
GPIO_C6	7	14	NC

	U6		
DATA_N	1	8	GPIO_C3
OUT_N	2	9	VCCO
GND	3	10	GPIO_C2
OUT_N	4	11	GPIO_C4
GND	5	12	DATA_P
NC	6	13	GND
GPIO_C1	7	14	NC

Micro USB Connector

U13	J24	
VCCO	1	5
USBD_N	2	6
USBD_P	3	7
NC	4	8

U6	J9	
VCCO	1	5
USBD_N	2	6
USBD_P	3	7
NC	4	8