SOC_NORF_HT3
Reference Manual

August 2019 ver1.2

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Revision History

Date	Rev	Comment
Nov 2017	v0	Initial version
Jul 2019	v1	Correct the flash socket pin
Jul 2019	v1.1	Add VRP、VRN and Jumper
Aug 2019	v1.2	Correct the flash part number

Contents

SOC_NORF_HT3

IMPORTANT!

ESD

The SOC_NORF_HT3 Transceiver Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

•Transport the card in an ESD bag

•Wear an anti-static wrist strap

•Make sure the work area is equipped with an ESD mat

Warning

Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS® system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

HapsTrak® 3 Connector Considerations

The HT3 connectors must be attached carefully! If connected improperly socket pins can be deformed or holding rail ends can become damaged.

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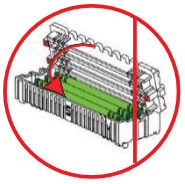

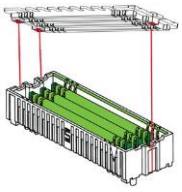

Overview

This document is the SOC_NORF_HT3 Reference Manual and describes the functions of the SOC_NORF_HT3 daughter board.

The SOC_NORF_HT3 daughter board may be set up to connect NOR-Flash through a HT3 connector.

SOC_NORF_HT3 daughter board consists of:

- 1 HT3 Connector, Power
- 1 TSOP56 Flash SOCKET
- 2 pairs of Differential MMCX Clock Connectors (for Global Clocks)

Figure 1: Top Views of SOC_NORF_HT3

Layout

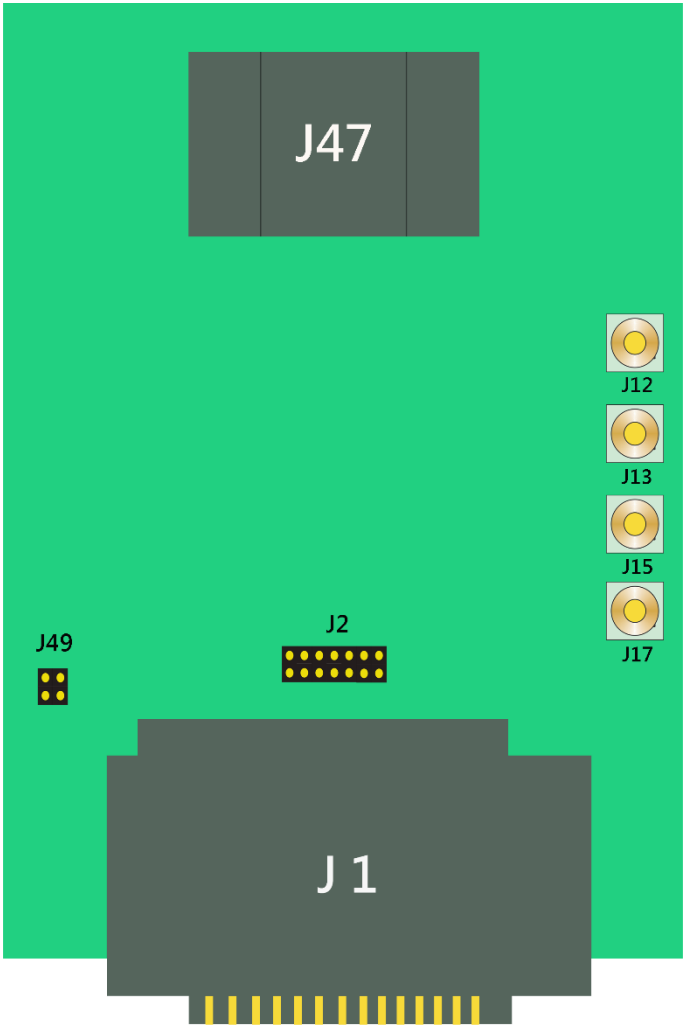

Figure 2: Top SOC_NORF_HT3 Layout

Block Diagram

Figure 3 shows the connectivity between the SOC_NORF_HT3 daughter board's NOR-Flash and connections to the HT3 connector. The HT3 I/O pin mapping is described in the J1 pin table on page 12.

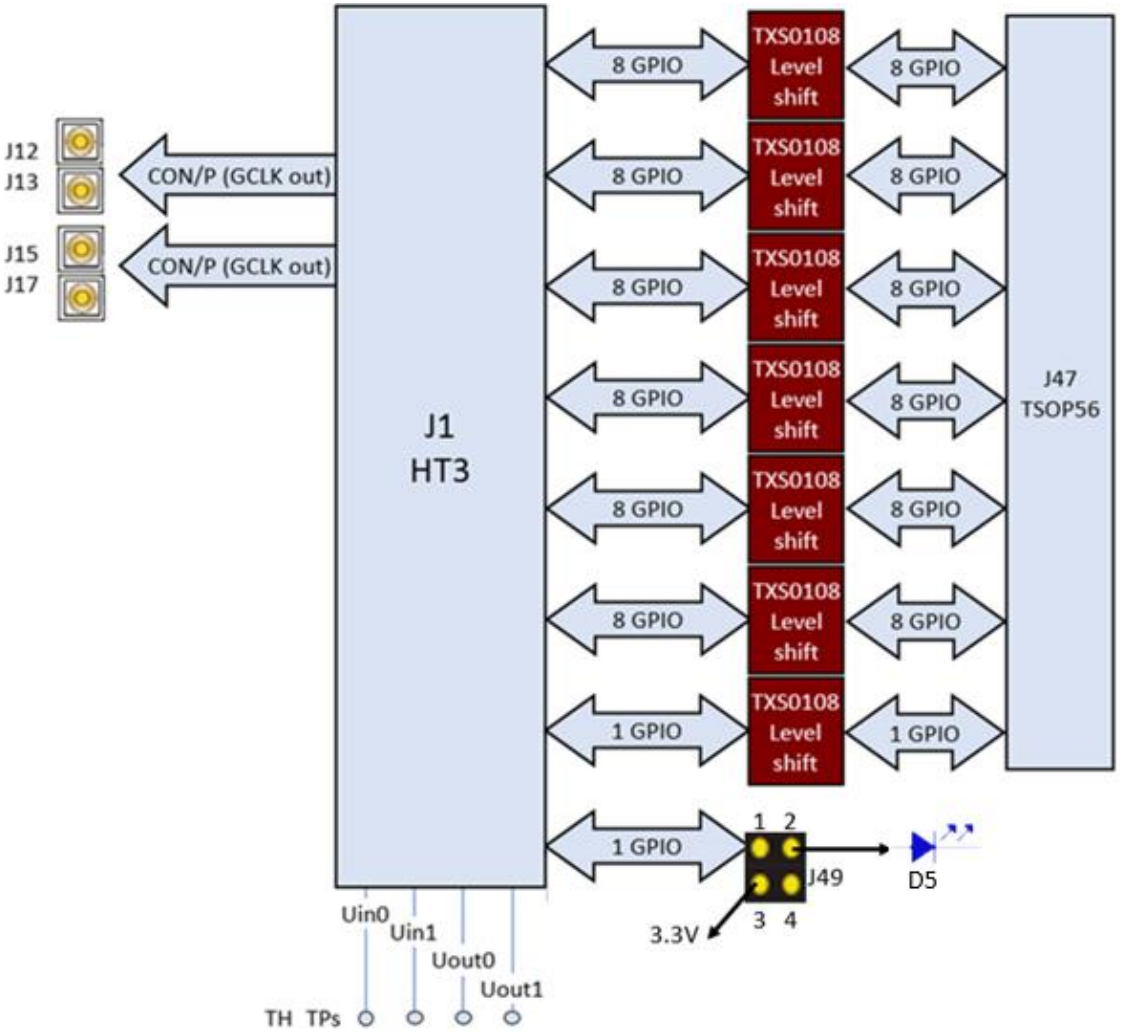

Figure 3: SOC_NORF_HT3 Block Diagram

Daughter Board Placement

HAPS-80 systems include 24 HT3 connectors for each FPGA. The Haps-Trak 3 (HT3) is a 160-pin connector containing 52 signal pins, most of which can be used for single ended or differential signaling. All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

The SOC_NORF_HT3 card connected to HAPS-80 through HT3 connector, Figure 4 is an example of board installed

Figure 4: SOC_NORF_HT3 mounted on HAPS-80 system

TSOP56 Flash SOCKET

The Flash socket J47 support 512 MB of non-volatile storage that can be used for configuration or software storage.

NOR Flash Part number: MT28EW512ABA

Supply voltage: 3.3V

Data path width: 16 bits (26 address lines and 7 control signals)

Jumper

Jumpers provide different configuration options dependent on the user requirements.

Jumper	Function
J49	Short Pin 1-2: FPGA detect GPIO_D12 being LOW, FPGA config the GPIO_A12 as output to control LED D5 Short Pin 3-4: FPGA detect GPIO_D12 being HIGH, FPGA config the GPIO_A12 as input

Table 1: Jumper Configuration Table

Clocks

MMCX connectors for clock connection between the user FPGA and other components in a hardware setup.

MMCX Connector		Direction	Source
J12/J13	Differential	Output	C0P/C0N
J15/J17	Differential	Output	C1P/C1N

Table 2: MMCX Clock Connections

Output Clocks

Output clocks are internal signals (FPGA generated clocks or HAPS global clocks) that travel from the HAPS system through the SOC_NORF_HT3 daughter board.

Access to the HAPS system's differential global clock (GCLK) signals are available through the Output clock SMB connector pairs on the SOC_NORF_HT3 daughter board. Table 1 is a list of clock connections for each MMCX connector.

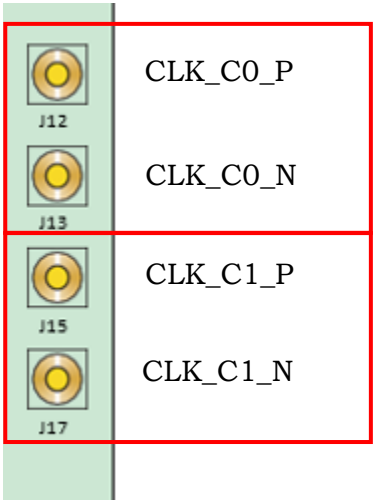

Figure 5: DIFF Clocks

Pin Tables

HT3 connector

J1								
(A0-B13)					(C0-C1P)			
Pin	Trace Name	Connector			Pin	Trace Name	Connector	
A0	NOR_A23	J47	3.3V		C0	NOR_A2	J47	3.3V
A1	NOR_A22				C1	NOR_A1		
A2	NOR_A15				C2	NOR_A24		
A3	NOR_A14				C3	NOR_CE_N		
A4	NOR_A13				C4	NOR_A16		
A5	NOR_A12				C5	NOR_BYTE_N		
A6	NOR_A11				C6	NOR_DQ15		
A7	NOR_A10				C7	NOR_DQ7		
A8	NOR_A9				C8	NOR_DQ14		
A9	NOR_A8				C9	NOR_DQ6		
A10	NOR_A19				C10	NOR_DQ13		
A11	NOR_A20				C11	NOR_DQ5		
A12	NOR_A25							
B0	NOR_WE_N	J47	3.3V		D0	NOR_DQ12	J47	3.3V
B1	NOR_RST_N				D1	NOR_DQ4		
B2	NOR_A21				D2	NOR_DQ11		
B3	NOR_WP_N				D3	NOR_DQ3		
B4	NOR_RY_BY_N				D4	NOR_DQ10		
B5	NOR_A18				D5	NOR_DQ2		
B6	NOR_A17				D6	NOR_DQ9		
B7	NOR_A7				D7	NOR_DQ1		
B8	NOR_A6				D8	NOR_DQ8		
B9	NOR_A5				D9	NOR_DQ0		
B10	NOR_A4				D10	NOROE_N		
B11	NOR_A3				D11	NOR_A0		
					D12	GPIO_D12	J49	3.3V

	J47 Flash
	J12/J13/J15/J17 Differential Clocks

C0N	CLK_C0_N	J13	VCCO	DIFF
C0P	CLK_C0_P	J12	VCCO	
C1N	CLK_C1_N	J17	VCCO	
C1P	CLK_C1_P	J15	VCCO	
VRP	VRP	J2	VCCO	
VRN	VRN	J2	VCCO	

Other-GPIO

J2			
-	1	2	-
-	3	4	-
-	5	6	-
-	7	8	-
-	9	10	-
-	11	12	-
GPIO_VRP	13	14	GPIO_VRN

TSOP56 Flash SOCKET

J47			
NOR_A [23]	1	56	NOR_A [24]
NOR_A [22]	2	55	NOR_A [25]
NOR_A [15]	3	54	NOR_A [16]
NOR_A [14]	4	53	NOR_BYTE#
NOR_A [13]	5	52	GND
NOR_A [12]	6	51	NOR_DQ [15]
NOR_A [11]	7	50	NOR_DQ [7]
NOR_A [10]	8	49	NOR_DQ [14]
NOR_A [9]	9	48	NOR_DQ [6]
NOR_A [8]	10	47	NOR_DQ [13]
NOR_A [19]	11	46	NOR_DQ [5]
NOR_A [20]	12	45	NOR_DQ [12]
NOR_WE#	13	44	NOR_DQ [4]
NOR_RST#	14	43	3.3V
NOR_A [21]	15	42	NOR_DQ [11]
NOR_WP#	16	41	NOR_DQ [3]
NOR_RY_BY#	17	40	NOR_DQ [10]
NOR_A [18]	18	39	NOR_DQ [2]
NOR_A [17]	19	38	NOR_DQ [9]
NOR_A [7]	20	37	NOR_DQ [1]
NOR_A [6]	21	36	NOR_DQ [8]
NOR_A [5]	22	35	NOR_DQ [0]
NOR_A [4]	23	34	NOR_OE#
NOR_A [3]	24	33	GND
NOR_A [2]	25	32	NOR_CE#
NOR_A [1]	26	31	NOR_A [0]
-	27	30	-
-	28	29	3.3V