SOC_SDNF_HT3
EH1704003014
Reference Manual

October 2019 ver1.1

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Revision History

Date	Rev	Comment
Nov 2017	v0	Initial version
Aug 2019	v1.0	Update the block diagram and Jumper
Oct 2019	v1.1	Correct the PMOD connector

Contents

SOC_SDNF_HT3

IMPORTANT!

ESD

The SOC_SOC_SDNF_HT3 Transceiver Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

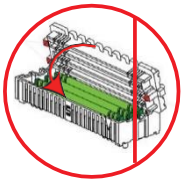
- Transport the card in an ESD bag
- Wear an anti-static wrist strap
- Make sure the work area is equipped with an ESD mat

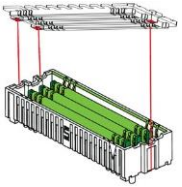
Warning

Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS® system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

HapsTrak® 3 Connector Considerations

The HT3 connectors must be attached carefully! If connected improperly socket pins can be deformed or holding rail ends can become damaged.





Overview

This document is the SOC_SDNF_HT3 Reference Manual and describes the functions of the SOC_SDNF_HT3 daughter board.

The SOC_SDNF_HT3 daughter board includes two micro-USB connectors providing RS-232 connections through a standard USB cable, connectivity for 20-pin ARM Cortex Debug interface, and a 12-pin PMOD connector with GPIO interface.

The SOC_SDNF_HT3 includes a secure digital input/output (SDIO) interface to provide user-logic access to a general purpose non-volatile SDIO memory card and peripherals. Onboard Flash socket (J47) provides an asynchronous data interface for high-performance I/O operations.

Figure 1: Top View of SOC_SDNF_HT3 daughter board.

SOC_SDNF_HT3 daughter board consists of:

- 1 20-pin ARM Cortex Debug + ETM Connector
- 1 12-pin PMOD Connector
- 2 Micro-USB Port
- 2 pairs of Differential MMCX Clock Connectors (for Global Clocks)
- 1 TSOP48 Flash Socket
- 1 SDIO Card Socket

Layout

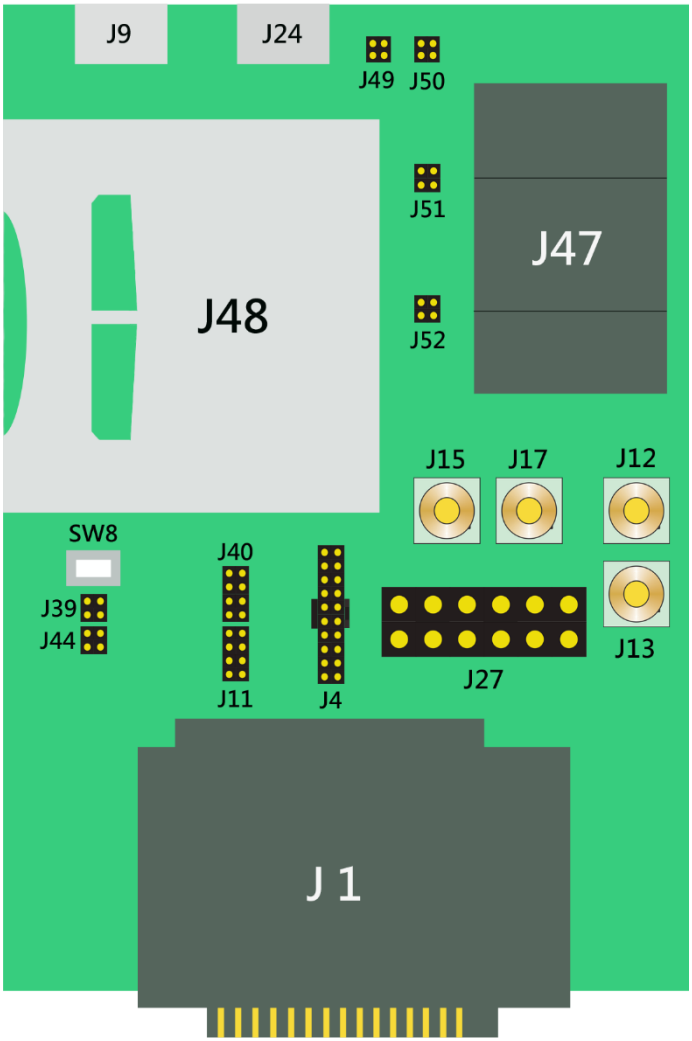


Figure 2: Top SOC_SDNF_HT3 Layout

Block Diagram

Figures 3 show the connectivity between the SOC_SDNF_HT3 daughter board's headers and connectors to the HT3 connector. The HT3 I/O pin mapping is described in the J1 pin table on page 16.

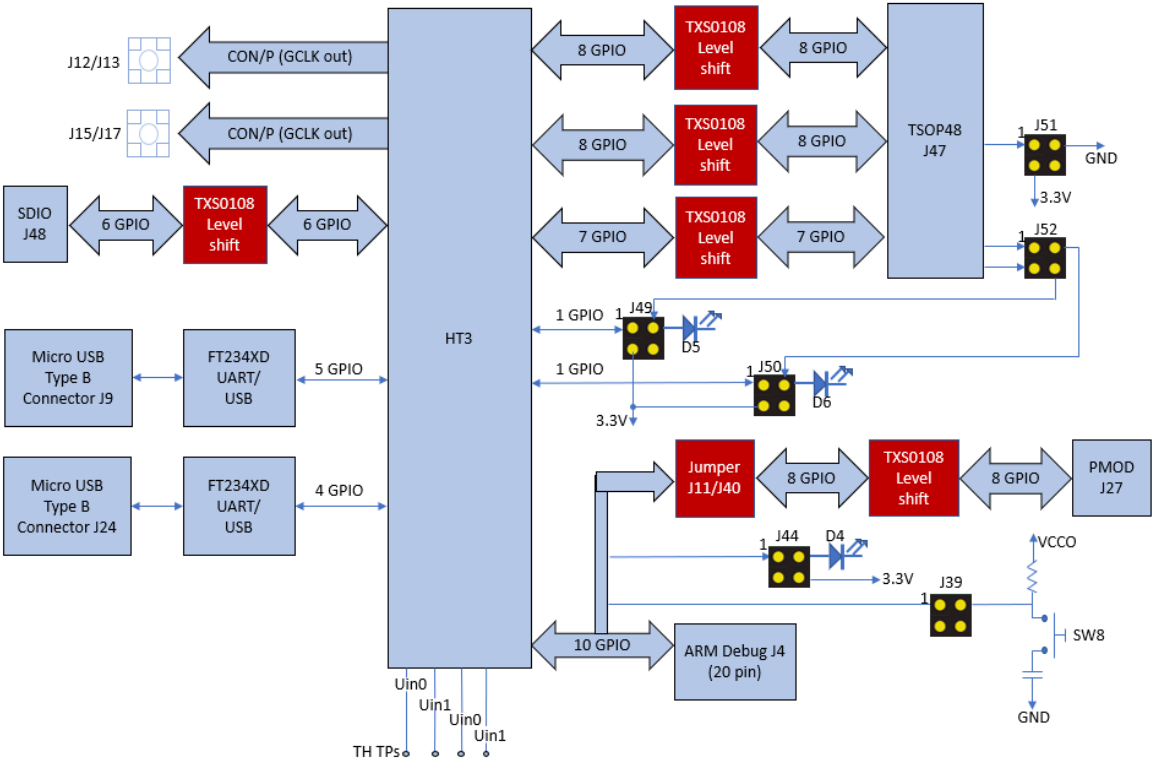


Figure 3: SOC_SDNF_HT3 Block Diagram

Daughter Board Placement

HAPS-80 systems include 24 HT3 connectors for each FPGA. The HapsTrak 3 (HT3) is a 160-pin connector containing 52 signal pins, most of which can be used for single ended or differential signaling. All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

The SOC_SDNF_HT3 card connected to HAPS-80 through HT3 connector, Figure 4 is an example of card installed.

Figure 4: SOC_SDNF_HT3 installed on a HAPS-80

HAPS GPIO Headers

Standard 3.3V GPIO Headers

Connector J27 is a standard 3.3V level HAPS GPIO header, which provides access to 12 FPGA I/O signals. The GPIO header is available for any design specific application including:

- Included LED/Button board
- I2C/SPI host adapter to access debug logic inside the FPGA (adapter cable may be required)
- PMOD module (adapter cable required for module connector for this board application)

High-Speed VCCO GPIO Headers

Special high-speed VCCO level GPIO headers (J11, J40) allow access to FPGA I/O signals at a VCCO level.

Tables 1 list various ways of connecting the control signals using jumper headers available on the SOC_SDNF_HT3 card

Control Pin	Jumper	Source Configuration
GPIO_D3	J11	Short Pin 1-2: Connector J27 Output pin 1
GPIO_D4	J11	Short Pin 3-4: Connector J27 Output pin 2
GPIO_D5	J11	Short Pin 5-6: Connector J27 Output pin 3
GPIO_D6	J11	Short Pin 7-8: Connector J27 Output pin 4
GPIO_D7	J40	Short Pin 1-2: Connector J27 Output pin 7
GPIO_D8	J40	Short Pin 3-4: Connector J27 Output pin 8
GPIO_D9	J40	Short Pin 5-6: Connector J27 Output pin 9
GPIO_D10	J40	Short Pin 7-8: Connector J27 Output pin 10

Table 1: SOC_SDNF_HT3 Control Signals

Jumpers

Jumpers provide different configuration options dependent on your requirements. The SDNF_HT3 has six 2x2 jumpers.

The header strip J39, J44, J49, J50, J51, J52 are populated by jumpers that connect the control signals (SWDCLK_TCLK, LED4, GPIO_D12, GPIO_A12, NANDFLSH_PIN38, NANDFLSH_PIN6 and NANDFLSH_PIN10) directly to HT3 I/O signals. If these signals are not used to generate the control signals, the pins can be accessed for design-specific use directly from headers J39, J44, J49, J50, J51, or J52.

Tables 2 lists various ways of connecting the control signals using jumper headers available on the SDNF_HT3 card

Jumper	Source Configuration	Remarks
J39	Short Pin 1-2: SWDCLK_TCLK connected to SW8 default high, press to set low	
J44	Short Pin 1-2: SDWIO_TMS to control LED4	
J49	Short Pin 1-2: GPIO_D12 as output to control LED5	
	Short Pin 1-3: GPIO_D12 as input being high	
J50	Short Pin 1-2: GPIO_A12 as output to control LED6	
	Short Pin 1-3: GPIO_A12 as input being high	
J51	Short Pin 1-2: NANDFLASH_PIN38 connected to GND	
	Short Pin 1-3: NANDFLASH_PIN38 connected to 3.3V	
J52	Short Pin 1-2: NANDFLASH_PIN6 connected to control LED5	When FPGA config the GPIO_D12/ GPIO_A12 as output to control LED, J52 should set to open
	Short Pin 3-4: NANDFLASH_PIN10 connected to control LED6	

Table 2: SDNF_HT3 Control Signals

ARM Debug Interface

SOC_SDNF_HT3 provides connectivity between connector J4 to user FPGA I/O pins through the HT3 connector. J4 is a 20-pin header with ground and signals arranged for ARM debug interface. Connect the proper signals in the user FPGA design from the FPGA internal ARM core debug ports to the HT3 pins according to the pin mapping depicted in the J1 pin table on page 17.

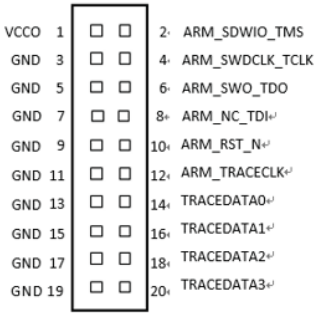


Figure 5: ARM 20-pin Cortex Debug + ETM Connector

Micro-USB Port

The micro-USB connector provides an RS-232 connection through a standard USB cable to your host computer. Designs that utilize an UART module may connect to the USB/UART pins to be accessed and controlled through a terminal application.

FTDI FX234XD is used to bridge UART and USB. Download and install the Virtual COM port (VCP) driver from www.ftdichip.com. The driver allows the USB device to appear as a COM port available to the host computer. Application software can access the USB device in the same way as it would access a standard COM port.

Part: USB to serial UART Interface
Number: FT234XD
Web address: ftdichip.com

Note: VCCO must be configured to 1.8V

Clocks

MMCX connectors for clock connections between the user FPGA and other components in a hardware setup.

Output Clocks

Output clocks are internal signals (FPGA generated clocks or HAPS global clocks) that travel from the HAPS system through the SOC_SDNF_HT3 daughter board.

Access to the HAPS system's differential global clock (GCLK) signals are available through the Output clock SMB connector pairs on the SOC_SDNF_HT3 daughter board. Table 3 is a list of clock connections for each MMCX connector.

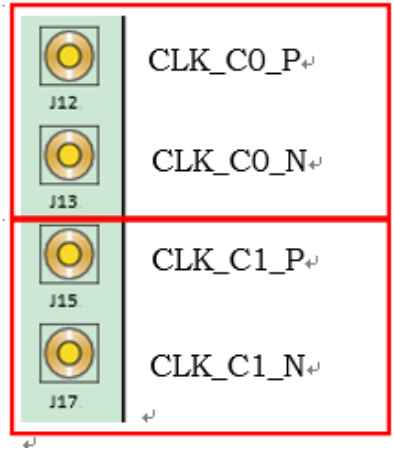


Figure 6: DIFF Clocks

MMCX Connector		Direction	Source
J12/J13	Differential	Output	C0P/C0N
J15/J17	Differential	Output	C1P/C1N

Table 3: MMCX Clock Connections

TSOP48 Flash Socket

The Flash socket J47 provide an asynchronous data interface for high-performance I/O operations.

Nand Flash Part number: MT29F4G08ABAEA

Device size: 4Gb: 4096 blocks

Page size x8

SDIO Card Socket

The SOC_SDNF_HT3 includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose nonvolatile SDIO memory cards and peripherals.

Pin Tables

HT3 Connector

J1							
(A0-B13)					(C0-C1P)		
Pin	Trace Name	Connector			Pin	Trace Name	Connector	
A0	NAND_IO[0]	J47	3.3V		C0	UART0_RTS_N	J24	VCCO
A1	NAND_IO[1]				C1	UART1_TXD	J9	
A2	NAND_IO[2]				C2	UART1_RXD		
A3	NAND_IO[3]				C3	UART1_RTS_N		
A4	NAND_IO[4]				C4	USRT1_CTS_N		
A5	NAND_IO[5]				C5	USRT1_SLEEP_N		
A6	NAND_IO[6]				C6	UART0_TXD	J24	
A7	NAND_IO[7]				C7	UART0_RXD		
A8	NAND_IO[8]				C8	SDIO_PIN1	J48	3.3V
A9	NAND_IO[9]				C9	SDIO_PIN2		
A10	NAND_IO[10]				C10	SDIO_PIN5		
A11	NAND_IO[11]				C11	SDIO_PIN7		
A12	GPIO_A12 / LED6	J50	3.3V					
B0	NAND_IO[12]	J47	3.3V		D0	UART0_CTSN	J24	VCCO
B1	NAND_IO[13]				D1	SDWIO_TMS	J4	VCCO
						LED4	J44	3.3V
B2	NAND_IO[14]				D2	SWDCLK_TCLK	J4	VCCO
						BUTTON	J39	3.3V
B3	NAND_IO[15]				D3	SWO_TDO	J4	VCCO
						PMOD_PIN1	J27	3.3V
B4	NAND_RB_N				D4	NC_TDI	J4	VCCO
						PMOD_PIN2	J27	3.3V
B5	NAND_RE_N				D5	ARM_RST_N	J4	VCCO
						PMOD_PIN3	J27	3.3V
B6	NAND_CE_N				D6	TRACECLK	J4	VCCO
						PMOD_PIN4	J27	3.3V
B7	NAND_CLE				D7	TRACEDATA_0	J4	VCCO
						PMOD_PIN7	J27	3.3V
B8	NAND_ALE				D8	TRACEDATA_1	J4	VCCO
						PMOD_PIN8	J27	3.3V
B9	NAND_WP_N				D9	TRACEDATA_2	J4	VCCO
						PMOD_PIN9	J27	3.3V
B10	NAND_WE_N				D10	TRACEDATA_3	J4	VCCO
						PMOD_PIN10	J27	3.3V
B11	SDIO_PIN8	J48	3.3V		D11	SDIO_PIN9	J48	3.3V
					D12	GPIO_D12 / LED5	J49	3.3V
					C0N	CLK_C0_N	J13	VCCO	DIFF
					C0P	CLK_C0_P	J12	VCCO	
					C1N	CLK_C1_N	J17	VCCO	
					C1P	CLK_C1_P	J15	VCCO	
					VRP	VRP	J2	VCCO	
					VRN	VRN	J2	VCCO	

	J47 Flash		J39/J44/J49/J50 Jumpers
	J9/J24 UART		
	J48 SDIO		J12/J13/J15/J17 Differential Clocks
	J4 ARM Debug		
	PMOD		

Other GPIO Connector

J2 Other-Signals			
-	1	2	-
-	3	4	-
-	5	6	-
-	7	8	-
-	9	10	-
-	11	12	-
GPIO_VRP	13	14	GPIO_VRN

TSOP48 Flash Socket

J47 NAND-Flash			
-	1	48	GND
-	2	47	IO 15
-	3	46	IO 14
-	4	45	IO 13
-	5	44	IO 7
NANDFLSH_PIN6	6	43	IO 6
R/B#	7	42	IO 5
RE#	8	41	IO 4
CE#	9	40	IO 12
NANDFLSH_PIN10	10	39	3.3V
-	11	38	NANDFLSH_PIN38
3.3V	12	37	3.3V
GND	13	36	GND
-	14	35	-
-	15	34	3.3V
CLE	16	33	IO 11
ALE	17	32	IO 3
WE#	18	31	IO 2
WP#	19	30	IO 1
-	20	29	IO 0
-	21	28	IO 10
-	22	27	IO 9
-	23	26	IO 8
-	24	25	GND

ARM Cortex Debug + ETM Connector

J4 ARM			
VCCO	1	2	SWDIO_TMS
GND	3	4	SWDCLK_TCLK
	5	6	SWO_TDO
	7	8	NC_TDI
	9	10	ARM_RST_N
	11	12	TRACECLK
	13	14	TRACEDATA[0]
	15	16	TRACEDATA[1]
	17	18	TRACEDATA[2]
	19	20	TRACEDATA[3]

SDIO Connector

J48 SDIO			
SDIO_PIN1	1	2	SDIO_PIN2
GND	3	4	3.3V
SDIO_PIN5	5	6	GND
SDIO_PIN7	7	8	SDIO_PIN8
SDIO_PIN9	9	10	GND
GND	11	12	GND
GND	13	14	GND
-	15	16	-
-	17	18	-

PMOD Connector

U15 3.3V	J27 3.3V		U15 3.3V
GPIO_D3	1	7	GPIO_D7
GPIO_D4	2	8	GPIO_D8
GPIO_D5	3	9	GPIO_D9
GPIO_D6	4	10	GPIO_D10
GND	5	11	GND
3.3V	6	12	3.3V

Jumpers

	J11 VCCO		U15 VCCO
GPIO_D3	1	2	GPIO_D3
GPIO_D4	3	4	GPIO_D4
GPIO_D5	5	6	GPIO_D5
GPIO_D6	7	8	GPIO_D6

	J40 VCCO		U15 VCCO
GPIO_D7	1	2	GPIO_D7
GPIO_D8	3	4	GPIO_D8
GPIO_D9	5	6	GPIO_D9
GPIO_D10	7	8	GPIO_D10

Jumper the J11 and J40 for PMOD output