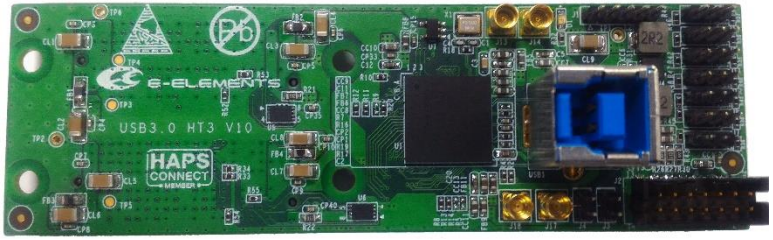
USB3_HT3

Reference Manual

October 2019 ver1.2



E-ELEMENTS

Copyright Notice and Proprietary Information

Third-Party Links

Any links to third-party websites included in this document are for your convenience only. E-elements does not endorse and is not responsible for such websites and their practices, including privacy practices, availability, and content.

E-ELEMENTS TECHNOLOGY CO., LTD.

5F, No.61, Lane76, RuiguangRd.,

Neihu Dist., Taipei,

Taiwan, R.O.C.

www.e-elements.com

Revision History

Date	Rev	Comment
Apr 2018	v0	Initial version
Aug 2019	v1.0	Correct the block diagram
Aug 2019	v1.1	Add VBUS mode description
Oct 2019	V1.2	Update the Diagram and J6-J12 default value

Contents

IMPORTANT!

ESD

The HAPS®USB3_HT3 Transceiver Card, as with all other electronic equipment, is sensitive to electrostatic discharge (ESD). When handling the transceiver card:

- Transport the card in an ESD bag
- Wear an anti-static wrist strap
- Make sure the work area is equipped with an ESD mat

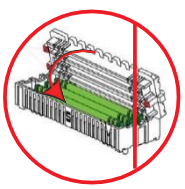
Warning

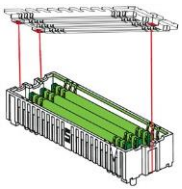
Never hot-plug interface cards, daughter boards or cables. Always power down the HAPS system when adding or removing a board, card, or cable to avoid damage to both the system and peripheral.

HapsTrak® 3 Connector Considerations

The HT3 connectors must be attached carefully! If connected improperly socket pins can be deformed or holding rail ends can become damaged.

When connecting daughter boards and HT3 cable connectors, they should be held parallel to the USB3_HT3 connector throughout the mating process.





Overview

USB3_HT3 is a Texas Instrument TUSB1310 based daughter board in the HAPS series providing a single port USB 3.0 Type-B connector. A SuperSpeed USB 3.0 Type A (F) to Type B (M) adapter is included for host mode. The daughter board provides a ULPI (UTMI + Low Pin) interface for USB 2.0 operation and a PIPE interface for USB 3.0 operation.

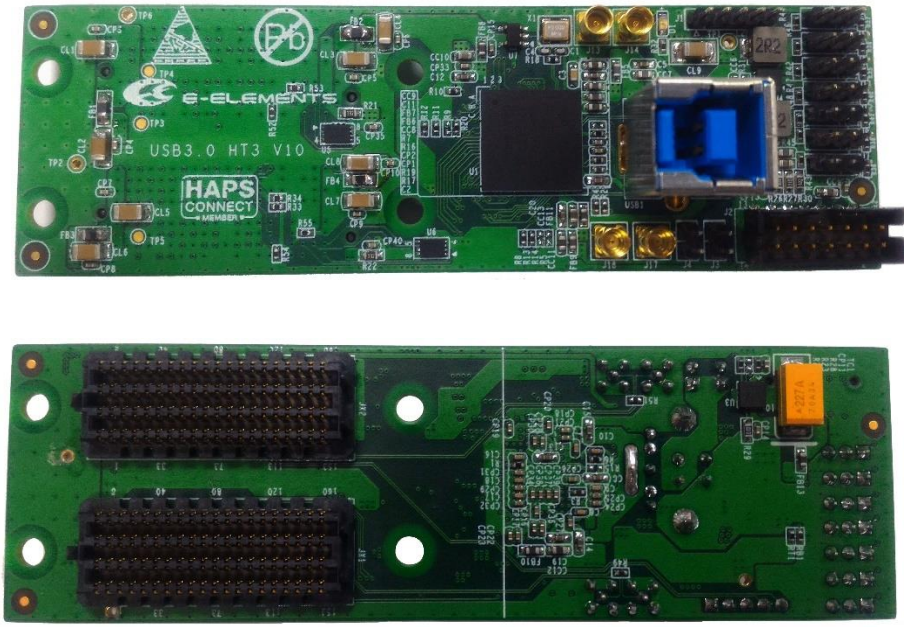


Figure 1: Top and Bottom View of USB3_HT3

USB3_HT3 daughter board consists of:

- 1 HAPS 14-pin GPIO Headers
- 1 HAPS 5-pin GPIO Headers
- 1 USB 3.0 Transceiver
- 1 USB 3.0 TYPE B Connector
- 2 HT3 Connectors
- 2 pairs of Differential MMCX Clock Connectors

Layout

Figure 2: Top and Bottom(dotted line) USB3_HT3 Card Layout

Card Placement

HAPS-80

HAPS-80 systems include 24 HT3 Connector for each FPGA. The Haps Trak 3 (HT3) is a 160-pin connector containing 52 signal pins, most of which can be used for single ended or differential signaling. All signals in a connector are associated with the same FPGA I/O bank voltage (VCCO). The I/O voltage dictates which electrical I/O standards can be used for the signal pins.

The USB3_HT3 card connected to HAPS-80 through two HT3 connectors, Figure 3 is the example of card installed

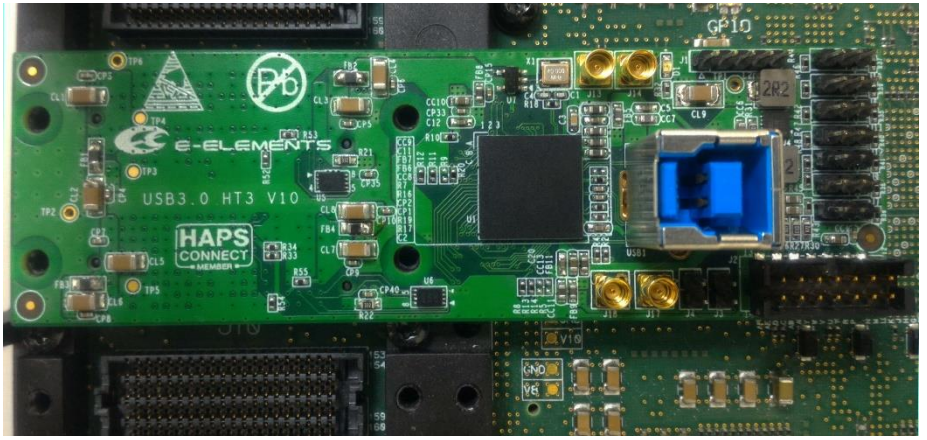


Figure 3: USB3_HT3 Card Installed on HAPS-80 system

Block Diagram

Figures 4 show the connectivity between the USB3_HT3 daughterboard's headers and connectors to the HT3 and USB3.0 connector. The following I/O block diagram in Figure 5 depicts how functional blocks are interconnected.

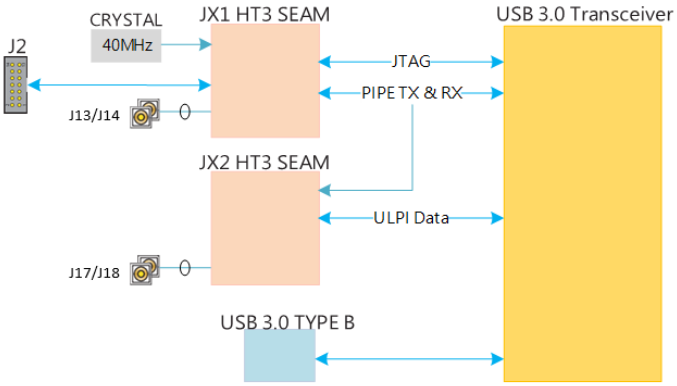


Figure 4: Block Diagram

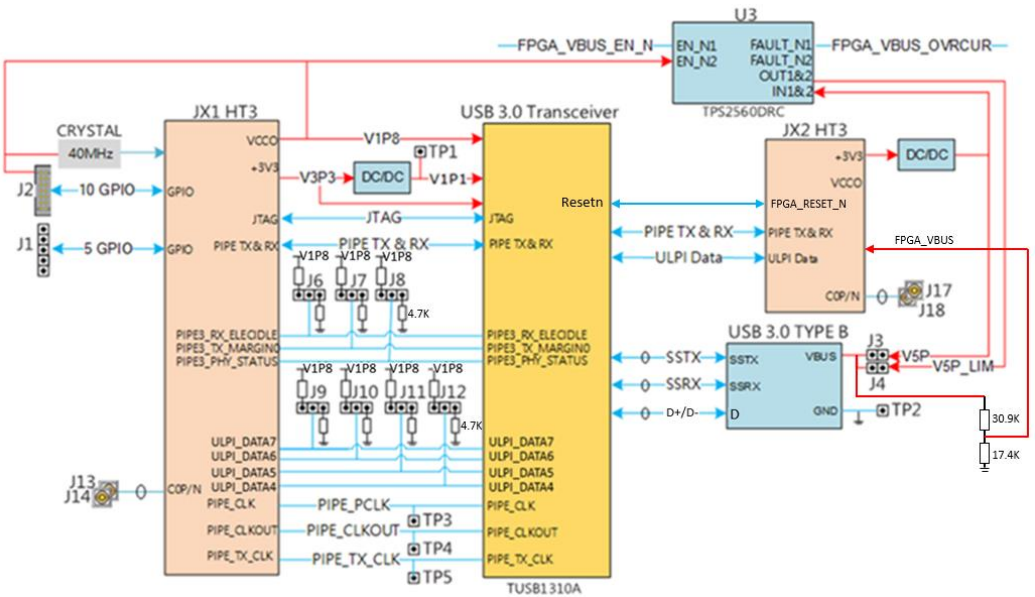


Figure 5: I/O Block Diagram

Modes

The USB3_HT3 can be used in either device or host mode. For host mode a jumper between pins 1 and 2 is used on J3 or J4. When short J3 and open J4, VBUS offer a power of 5V/1.8A. When short J4 and open J3, VBUS offer a Current-limited power of 5V/0.56A. J3 and J4 jumper short together is not allowed. For device mode disconnect a wire between pins 1 and 2 on J3 and J4.

Mode	J3	J4
Host	short	short
Device	open	open

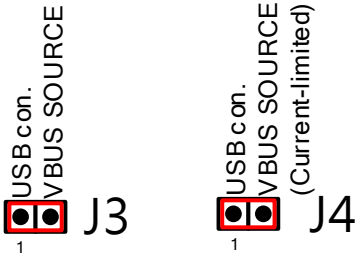


Figure 6: USB3 mode configuration

VBUS Handling

Select the local +5 V rail to use for VBUS logic with the J3 or J4 jumper.

	VBUS Source Selection
J3 Pins 1-2	Local +5 V
J4 Pins 1-2	Local +5 V with Current-limited

Table 1: VBUS Source Selection

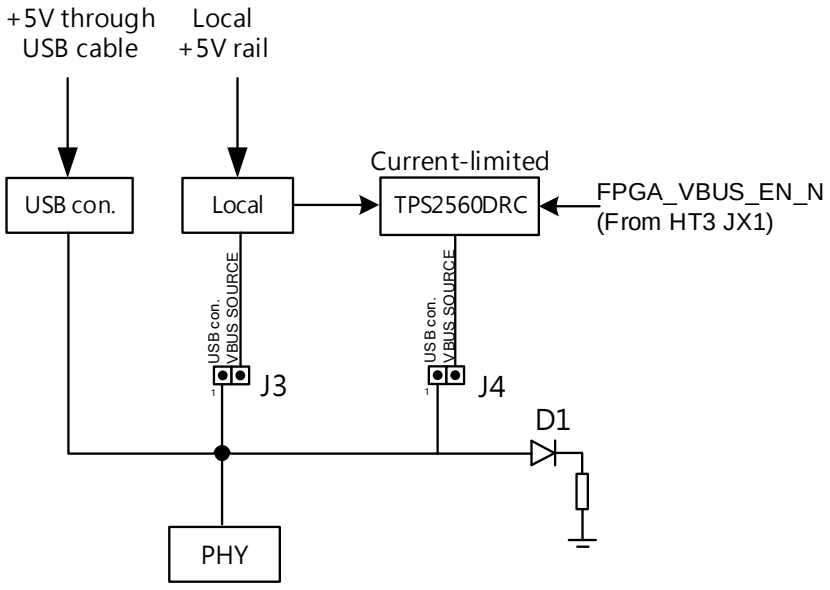


Figure 7: VBUS Handling

HAPS GPIO Headers

Standard VCCO GPIO Headers

Connectors J1 and J2 is standard VCCO level HAPS GPIO Headers. The I/O pins mapping are described on page 18.

The GPIO headers are available for any design specific application including:

- Included LED/Button board
- I2C/SPI host adapter to access debug logic inside the FPGA (adapter cable may be required)
- Pmod modules (adapter cable required for module connectors)

Part Number: J1: PH1X5-2MM J2: 87832-142

Jumpers and Headers

Jumpers provide different configuration options dependent on the user requirements. The USB3_HT3 has Seven 1x3 jumpers, two 1x2 jumpers. Refer to the I/O Block Diagram in Figure 5, on page 10.

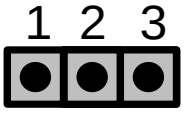
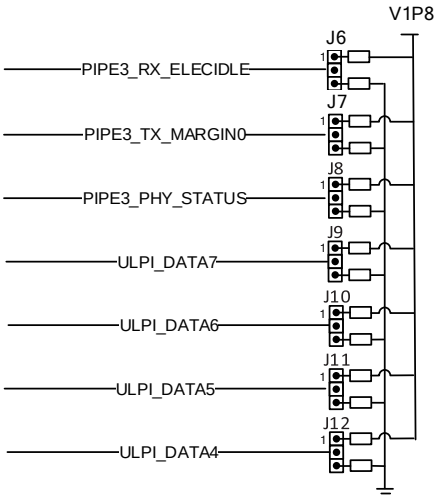


Figure 8: Header Strip

J6-J12 is populated by jumpers that connect pull-up or pull-down Resistor for the signal directly to HT3 I/O signals and USB3.0.

Signal	Jumper	Description	Configuration	Default
PIPE3_RX_ELECIDLE	J6	0: Crystal Input 1: Clock Input	Short Pin 1-2: Pull Up Short Pin 2-3: Pull Down	Pull Down
PIPE3_TX_MARGIN0	J7	0: Spread spectrum clocking enable 1: Spread spectrum clocking disable	Short Pin 1-2: Pull Up Short Pin 2-3: Pull Down	Pull Down
PIPE3_PHY_STATUS	J8	0: 16-bit PIPE SDR mode Must be set 0 at reset	Short Pin 1-2: Pull Up Short Pin 2-3: Pull Down	Pull Down
ULPI_DATA7	J9	0: Starts transmitting packet data 1: Puts PIPE into isolate mode	Short Pin 1-2: Pull Up Short Pin 2-3: Pull Down	Pull Down
ULPI_DATA6	J10	0: 8-bit ULPI SDR mode Must be set 0 at reset	Short Pin 1-2: Pull Up Short Pin 2-3: Pull Down	Pull Down
ULPI_DATA5 ULPI_DATA4	J11 J12	00: 20 MHz on XI 01: 25 MHz on XI 10: 30 MHz on XI 11: 40 MHz on XI	Short Pin 1-2: Pull Up Short Pin 2-3: Pull Down	Pull Up Pull Up

Table 2: J6-J12 Jumpers for Pull Up or Down



VBUS Handling

J3-J4 is populated by jumpers that connect VBUS of USB1 to 5V. Refer to the VBUS Handling and in Figure 7, on page 12.

Clocks

MMCX connectors for clock connections between the user FPGA and other components in a hardware setup.

Output Clocks

Output clocks are internal signals (FPGA generated clocks or HAPS global clocks) that travel from the HAPS system through the USB3_HT3 daughter board.

Access to the HAPS system's differential global clock (GCLK) signals are available through the Output clock SMB connector pairs on the USB3_HT3 daughter board. Table 3 is a list of clock connections for each MMCX connector.

MMCX Connector	Differential or Single- ended	Direction	Source or Destination	
J13/J14	DIFF	Output	Source	HT3
J17/J18	DIFF	Output		HT3

Table 3: MMCX Clock Connections

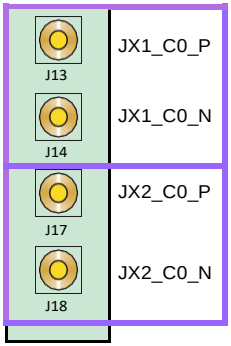


Figure 9: DIFF Clocks

Pin Table

HT3 Connectors

JX1

JX1						
(A0-B13)				(C0-C1P)		
Pin	Trace Name	Connector		Pin	Trace Name	Connector
A0	PIPE3_PCLK	U1		C0	PIPE3_RX_DATA5	U1
A1	JTAG_TRSTN			C1	PIPE3_RX_DATA8	
A2	PIPE3_RX_DATA0			C2	PIPE3_RX_DATA6	
A3	PIPE3_PHY_STATUS			C3	PIPE3_RX_DATA7	
A4	JTAG_TMS			C4	PIPE3_RX_DATA10	
A5	JTAG_TDO			C5	PIPE3_RX_DATA11	
A6	JTAG_TDI			C6	PIPE3_RX_DATA9	
A7	JTAG_TCK			C7	PIPE3_RX_DATAK0	
A8	JX1_A8	J2		C8	PIPE3_RX_DATA12	
A9	JX1_A9			C9	PIPE3_RX_DATA15	
A10	PIPE3_RX_VALID	U1		C10	PIPE3_RX_DATA13	
A11	PIPE3_RX_ELECIDLE			C11	PIPE3_RX_DATA14	
A12	JX1_A12	J2		C12	-	
A13	-			C13	-	
B0	PIPE3_CLKOUT	U1		D0	CRYSTAL_OUT	U7
B1	PIPE3_RX_DATA2			D1	JX1_D1	J2
B2	PIPE3_RX_DATA3			D2	JX1_D2	
B3	PIPE3_RX_DATA4			D3	JX1_D3	
B4	PIPE3_RX_DATA1			D4	JX1_D4	
B5	PIPE3_RX_TERMINATION			D5	JX1_D5	
B6	PIPE3_RX_STATUS0			D6	JX1_D6	
B7	PIPE3_RX_STATUS1			D7	JX1_D7	
B8	PIPE3_RX_POLARITY			D8	FPGA_VBUS_EN_N	U3
B9	PIPE3_ELAS_BUF_MODE			D9	FPGA_VBUS_OVRCUR	
B10	PIPE3_RX_STATUS2			D10	JX1_D10	J1
B11	PIPE3_RX_DATAK1			D11	JX1_D11	
B12				D12	JX1_D12	
B13				D13	-	
				C0N	JX1_C0P	J13 DIFF
				C0P	JX1_C0N	J14
				C1N	-	
				C1P	-	

	U1 USB 3.0 Transceiver
	J1/J2 GPIO header
	J13/J14 Differential Clocks
	U1 VBUS Current-limited

JX2

JX2						
(A0-B13)				(C0-C1P)		
Pin	Trace Name	Connector		Pin	Trace Name	Connector
A0	PIPE3_TX_DATA13	U1		C0	PIPE3_TX_DATA8	U1
A1	PIPE3_TX_DATA14			C1	PIPE3_TX_DATA9	
A2	PIPE3_TX_CLK			C2	ULPI_DATA7	
A3	PIPE3_TX_ELECIDLE			C3	ULPI_DATA5	
A4	PIPE3_TX_DATAK1			C4	PIPE3_TX_ONESZEROS	
A5	PIPE3_TX_DATA15			C5	PIPE3_TX_SWING	
A6	PIPE3_TX_DATAK0			C6	ULPI_DATA3	
A7	PIPE3_TX_DATA12			C7	ULPI_DATA0	
A8	PIPE3_POWER_DOWN0			C8	PIPE3_TX_DETRX_LPBK	
A9	PIPE3_POWER_DOWN1			C9	ULPI_DIR	
A10	PIPE3_PHY_RESET_N			C10	ULPI_NXT	
A11	FPGA_RESET_N			C11	FPGA_VBUS	
A12	JX2_A12	J1		C12	-	
A13	-			C13	-	
B0	ULPI_CLK	U1		D0	PIPE3_TX_DATA7	U1
B1	PIPE3_RATE			D1	PIPE3_TX_DATA5	
B2	PIPE3_TX_DATA10			D2	PIPE3_TX_DATA6	
B3	PIPE3_TX_DATA11			D3	PIPE3_TX_DATA4	
B4	OUT_ENABLE			D4	PIPE3_TX_DATA3	
B5	PIPE3_TX_DEEMPH0			D5	PIPE3_TX_DATA1	
B6	ULPI_STP			D6	PIPE3_TX_DATA2	
B7	PIPE3_TX_MARGIN0			D7	PIPE3_TX_DATA0	
B8	PIPE3_TX_DEEMPH1			D8	ULPI_DATA2	
B9	PIPE3_PWRPRESENT			D9	ULPI_DATA1	
B10	PIPE3_TX_MARGIN1			D10	ULPI_DATA6	
B11	PIPE3_TX_MARGIN2			D11	ULPI_DATA4	
B12				D12	JX2_D12	J1
B13				D13	-	
				C0N	JX2_C0P	J17
				C0P	JX2_C0N	J18
				C1N	-	
				C1P	-	

	U1 USB 3.0 Transceiver
	J1 GPIO header
	J17/J18 Differential Clocks

USB1

U1

Pin	Trace Name
1	VBUS
2	DM_ULPI
3	DP_ULPI
4	GND
5	SSTXN
6	SSTXP
7	GND
8	SSRXN
9	SSRXP

GPIO Connectors

J1

Pin	Trace Name
1	JX1_D10
2	JX1_D11
3	JX1_D12
4	JX2_A12
5	JX2_D12

J2

Pin	Trace Name
1	+1V8
2	+1V8
3	JX1_A9
4	JX1_A8
5	JX1_D1
6	JX1_A12
7	JX1_D3
8	JX1_D2
9	JX1_D5
10	JX1_D4
11	JX1_D7
12	JX1_D6
13	GND
14	GND